EXHIBIT AA

US007148111B2

(12) **United States Patent**
Mo et al.

(10) **Patent No.: US 7,148,111 B2**
(45) **Date of Patent: *Dec. 12, 2006**

(54) **METHOD OF MANUFACTURING A TRENCH TRANSISTOR HAVING A HEAVY BODY REGION**

(75) Inventors: **Brian Sze-Ki Mo**, Fremont, CA (US); **Duc Chau**, San Jose, CA (US); **Steven Sapp**, Felton, CA (US); **Izak Bencuya**, Saratoga, CA (US); **Dean E. Probst**, West Jordan, UT (US)

(73) Assignee: **Fairchild Semiconductor Corporation**, San Jose, CA (US)

(*) Notice: Subject to any disclaimer, the term of this patent is extended or adjusted under 35 U.S.C. 154(b) by 0 days.

This patent is subject to a terminal disclaimer.

(21) Appl. No.: **10/927,788**

(22) Filed: **Aug. 27, 2004**

(65) **Prior Publication Data**

US 2005/0079676 A1 Apr. 14, 2005

Related U.S. Application Data

(60) Continuation of application No. 10/347,254, filed on Jan. 17, 2003, now Pat. No. 6,828,195, which is a continuation of application No. 09/854,102, filed on May 9, 2001, now Pat. No. 6,521,497, which is a division of application No. 08/970,221, filed on Nov. 14, 1997, now Pat. No. 6,429,481.

(51) **Int. Cl.**
H01L 21/336 (2006.01)

(52) **U.S. Cl.** **438/270**; 438/272; 438/589

(58) **Field of Classification Search** 438/270, 438/272, 589

See application file for complete search history.

(56) **References Cited**

U.S. PATENT DOCUMENTS

4,070,690	A	1/1978	Wickstrom
4,132,998	A	1/1979	Dingwall
4,145,703	A	3/1979	Blanchard et al.
4,326,332	A	4/1982	Kenney
4,329,705	A	5/1982	Baker
4,344,081	A	8/1982	Pao et al.
4,345,265	A	8/1982	Blanchard
4,398,339	A	8/1983	Blanchard et al.

(Continued)

FOREIGN PATENT DOCUMENTS

CN	1090680	9/1994

(Continued)

OTHER PUBLICATIONS

Blanchard, Richard A., "Optimization of Discrete High Power MOS Transistors," Stanford Electronics Laboratory, Integrated Circuits Laboratory, Technical Report No. IDEZ696-2 (Apr. 1982).

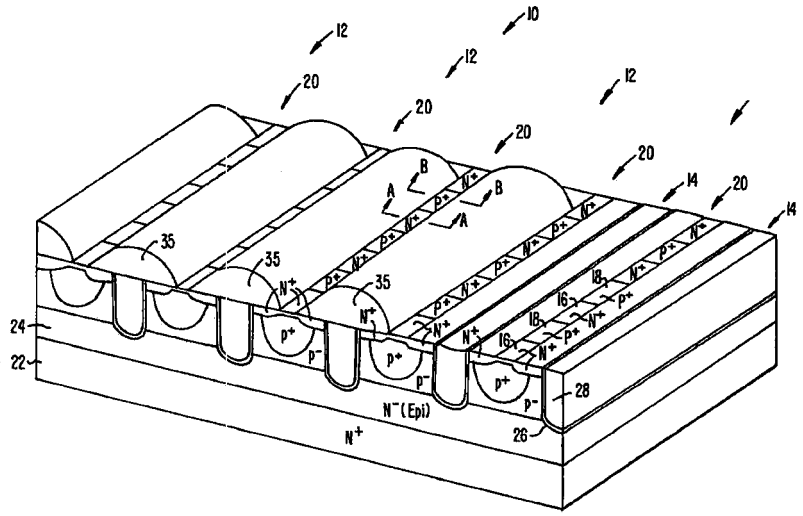
(Continued)

Primary Examiner—Lynne A. Gurley
(74) *Attorney, Agent, or Firm*—Babak S. Sani; Townsend and Townsend and Crew LLP

(57) **ABSTRACT**

A trenched field effect transistor is provided that includes (a) a semiconductor substrate, (b) a trench extending a predetermined depth into the semiconductor substrate, (c) a pair of doped source junctions, positioned on opposite sides of the trench, (d) a doped heavy body positioned adjacent each source junction on the opposite side of the source junction from the trench, the deepest portion of the heavy body extending less deeply into said semiconductor substrate than the predetermined depth of the trench, and (e) a doped well surrounding the heavy body beneath the heavy body.

36 Claims, 9 Drawing Sheets



U.S. PATENT DOCUMENTS

4,503,449	A		3/1985	David et al.
4,503,598	A		3/1985	Vora et al.
4,541,001	A		9/1985	Schutten et al.
4,639,762	A		1/1987	Neilson et al.
4,682,405	A		7/1987	Blanchard et al.
4,683,643	A		8/1987	Nakajima et al.
4,767,722	A		8/1988	Blanchard
4,808,543	A		2/1989	Parrillo et al.
4,845,537	A		7/1989	Nishimura et al.
4,860,072	A		8/1989	Zommer
4,881,105	A		11/1989	Davari et al.
4,893,160	A		1/1990	Blanchard
4,914,058	A		4/1990	Blanchard
4,967,245	A		10/1990	Cogan et al.
4,983,535	A		1/1991	Blanchard
5,016,068	A		5/1991	Mori
5,017,504	A		5/1991	Nishimura et al.
5,045,900	A		9/1991	Tamagawa
5,072,266	A		12/1991	Bulucea et al.
5,124,764	A		6/1992	Mori
5,160,491	A		11/1992	Mori
5,168,331	A		12/1992	Yilmaz
5,298,442	A		3/1994	Bulucea et al.
5,298,780	A		3/1994	Harada
5,316,959	A		5/1994	Kwan et al.
5,321,289	A		6/1994	Baba et al.
5,341,011	A		8/1994	Hshieh et al.
5,405,794	A		4/1995	Kim
5,410,170	A		4/1995	Bulucea et al.
5,430,324	A		7/1995	Bencuya
5,455,190	A		10/1995	Hsu
5,460,985	A		10/1995	Tokura et al.
5,468,982	A		11/1995	Hshieh et al.
5,474,943	A		12/1995	Hshieh et al.
5,508,534	A		4/1996	Nakamura et al.
5,532,179	A		7/1996	Chang et al.
5,541,425	A		7/1996	Nishihara
5,558,313	A		9/1996	Hshieh et al.
5,567,634	A		10/1996	Herbert et al.
5,578,851	A		11/1996	Hshieh et al.
5,592,005	A		1/1997	Floyd et al.
5,597,765	A		1/1997	Yilmaz et al.
5,602,046	A		2/1997	Calafut et al.
5,605,852	A		2/1997	Bencuya
5,614,751	A		3/1997	Yilmaz et al.
5,629,543	A		5/1997	Hshieh et al.
5,639,676	A		6/1997	Hshieh et al.
5,648,670	A		7/1997	Blanchard
5,661,322	A		8/1997	Williams et al.
5,665,619	A	*	9/1997	Kwan et al. 438/270
5,665,996	A		9/1997	Williams et al.
5,674,766	A		10/1997	Darwish et al.
5,679,966	A		10/1997	Baliga et al.
5,688,725	A		11/1997	Darwish et al.
5,689,128	A		11/1997	Hshieh et al.
5,701,026	A		12/1997	Fushima et al.
5,763,915	A		6/1998	Hshieh et al.
5,767,550	A		6/1998	Calafut et al.
5,776,812	A		7/1998	Takahashi et al.
5,780,324	A		7/1998	Tokura et al.
5,783,491	A		7/1998	Nakamura et al.
5,783,915	A		7/1998	Shida et al.
5,801,408	A		9/1998	Takahashi
5,814,858	A		9/1998	Williams
5,864,159	A	*	1/1999	Takahashi 257/330
5,879,971	A		3/1999	Witek
5,895,952	A		4/1999	Darwish et al.
5,930,630	A		7/1999	Hshieh et al.
5,986,304	A		11/1999	Hshieh et al.
5,998,836	A		12/1999	Williams
5,998,837	A		12/1999	Williams
6,015,737	A		1/2000	Tokura et al.
6,049,108	A		4/2000	Williams et al.
6,121,089	A		9/2000	Zeng et al.
6,204,533	B1		3/2001	Williams et al.
6,221,721	B1	*	4/2001	Takahashi 438/270
6,368,920	B1	*	4/2002	Beasom 438/270
6,426,260	B1	*	7/2002	Hshieh 438/270
6,429,481	B1		8/2002	Mo et al.
6,521,497	B1	*	2/2003	Mo 438/270
6,710,406	B1		3/2004	Mo et al.
6,828,195	B1	*	12/2004	Mo et al. 438/270
2002/0185679	A1		12/2002	Baliga

FOREIGN PATENT DOCUMENTS

EP	0238749	9/1987
EP	0550770	7/1993
EP	0583028	2/1994
EP	0698919	2/1996
EP	0720235	3/1996
EP	0720236	3/1996
EP	0720236	7/1996
EP	0746030	12/1996
EP	0755076	1/1997
EP	0795911	9/1997
EP	0801425	10/1997
GB	2269050	1/1994
JP	56131960	10/1981
JP	57018365	1/1982
JP	57153469	9/1982
JP	58137254	8/1983
JP	58210678	12/1983
JP	59080970	5/1984
JP	59193064	11/1984
JP	60028271	2/1985
JP	61102782	5/1986
JP	62012167	1/1987
JP	62016572	1/1987
JP	62023171	1/1987
JP	62046569	2/1987
JP	63114173	5/1988
JP	05226661	9/1993
JP	08204194	8/1996
JP	08250731	9/1996
JP	08316479	11/1996
JP	09036362	2/1997
JP	09102607	4/1997
JP	09270512	10/1997
WO	WO 93/03502	2/1993
WO	WO 95/34094	12/1995
WO	WO 97/07547	2/1997
WO	WO 97/16853	5/1997

OTHER PUBLICATIONS

Chang, T.S., et al, "Vertical FET Randon-Access Memories with Deep Trench Isolation," IBM Technical Disclosure Bulletin, pp. 3683-3687 (Jan. 1980).

Goodenough, Frank et al. "Tech Insights Enables Portable Power Control", Electronic Design, Apr. 14, 1997.

Grant, D.A. et al., "Power Mosfets: Theory and Applications," A. Wiley-Interscience Publication COPYRGT. 1989, pp. 5-23. [ISBN 0-471-82867-X].

Homes, F. E. et al., "V Groove M.O.S. Transistor Technology," Electronic letters vol. 9, No. 19, pp. 457-458 (Sep. 20, 1973).

Homes, F. E. et al., "VMOS—A New MOS Integrated Circuit Technology," Solid-State Electronics, vol. 17, pp. 791-797 (1974).

Lidow, A. et al. "Power Mosfet Technology," Lidow et al., (International Electron Devices meeting, Dec. 3-5, 1979, IEAM Technical Digest, pp. 79-83.

Lisiak, Kenneth P.; Berger, Josef. "Optimization of Nonplanar Power MOS Transistors," IEE Transactions on Electron Devices, vol. ED-25, No. 10, pp. 1229-1234 (Oct. 1978).

Ou-Yang, Paul, "Double Ion Implanted V-MOS Technology," IEEE Journal of Solid-State Circuits, vol. SC-12, No. 1, pp. 3-10 (Feb. 1977).

"Optimization of Nonplanar Power MOS Transistors," Lisiak et al., IEEE Transactions of Electron Devices, vol. ED-25, No. 10, Oct. 1975, pp. 1229-1234.

Salama, C. Andre; Oakes, James G., "Nonplanar Power Field-Effect Transistor," IEEE Transactions on Electron Devices, vol. ED-25, No. 10, pp. 1222-1228 (Oct. 1978).

Sun, S. C., "Physics and Technology of Power MOSFETs," Stanford Electronics Laboratory, Integrated Circuits Laboratory, Technical Report No. IDEZ696-1 (Feb. 1982).

Sze, S. M., "P-N-Junction Diode" Physics of Semiconductor Devices Second Edition Bell Laboratories, pp. 63-108 (1981).

* cited by examiner

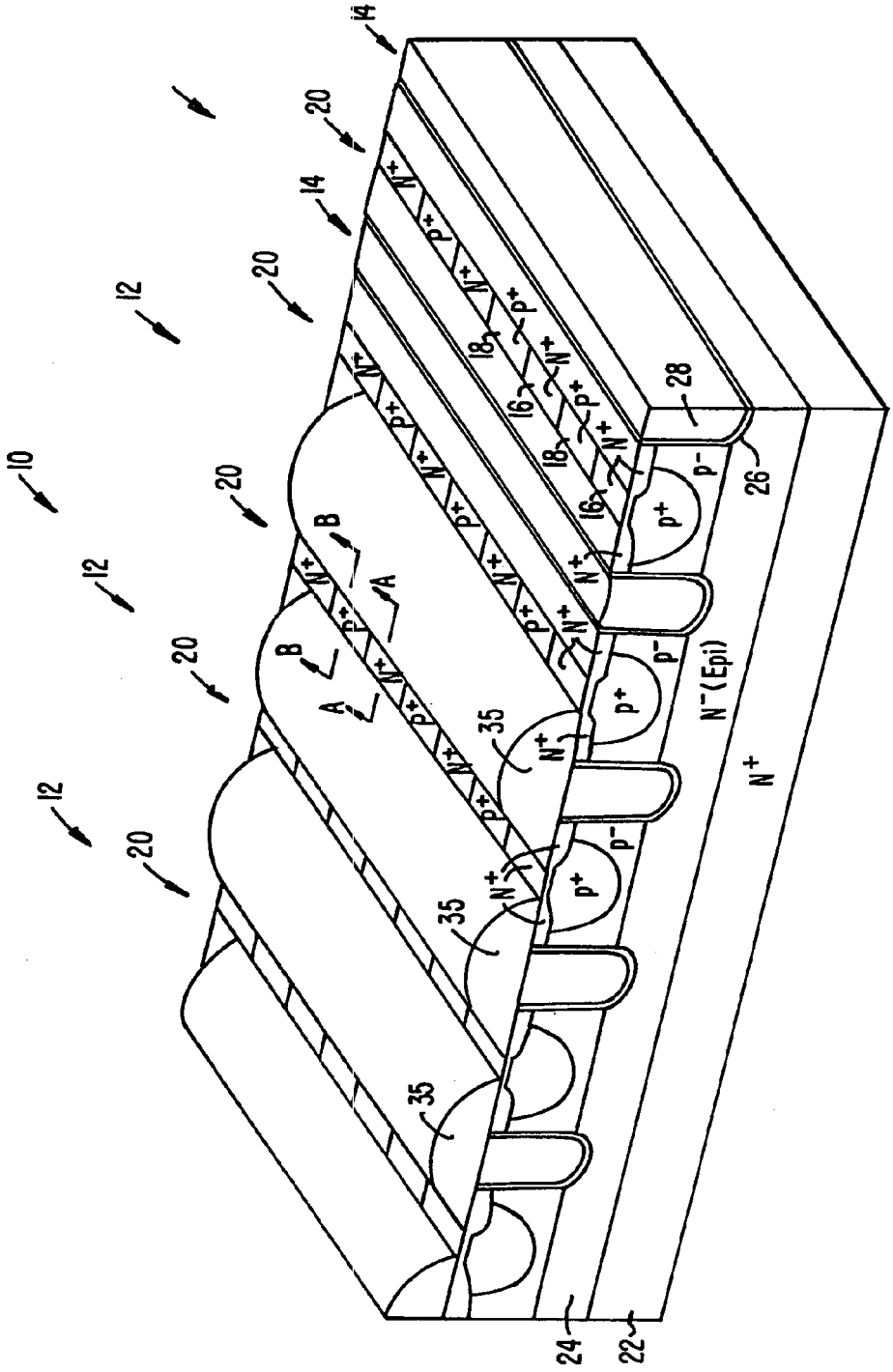


FIG. 1.

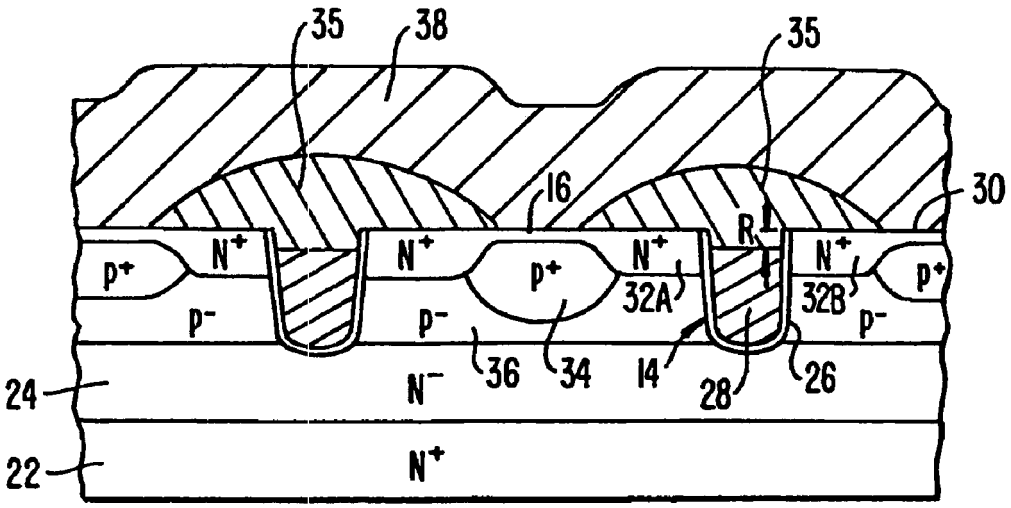

35
38
35
16
30
R1
N+
N+
N+
N+
p+
p+
p+
32A
32B
p-
p-
p-
36
34
14
28
26
24
N-
22
N+

FIG. 1A.

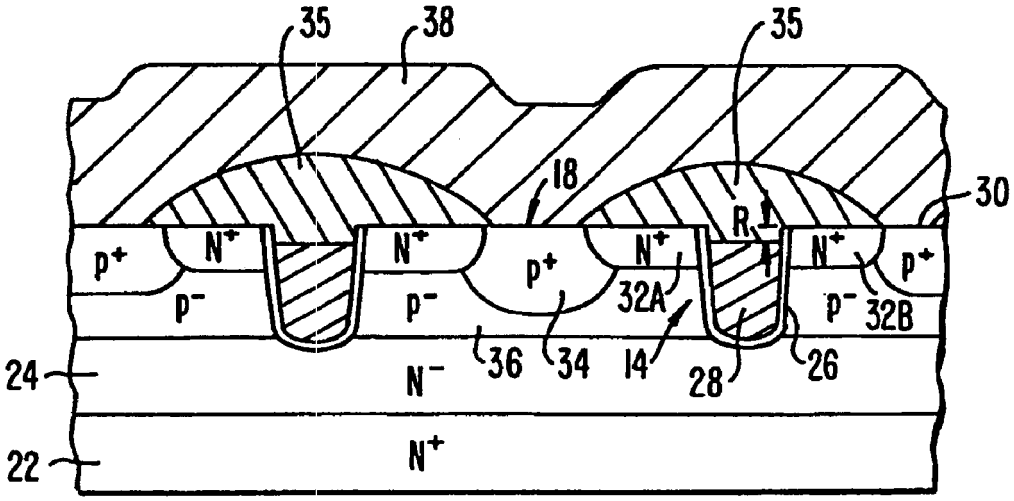

35
38
35
18
30
R1
N+
N+
N+
N+
p+
p+
p+
32A
32B
p-
p-
p-
36
34
14
28
26
24
N-
22
N+

FIG. 1B.

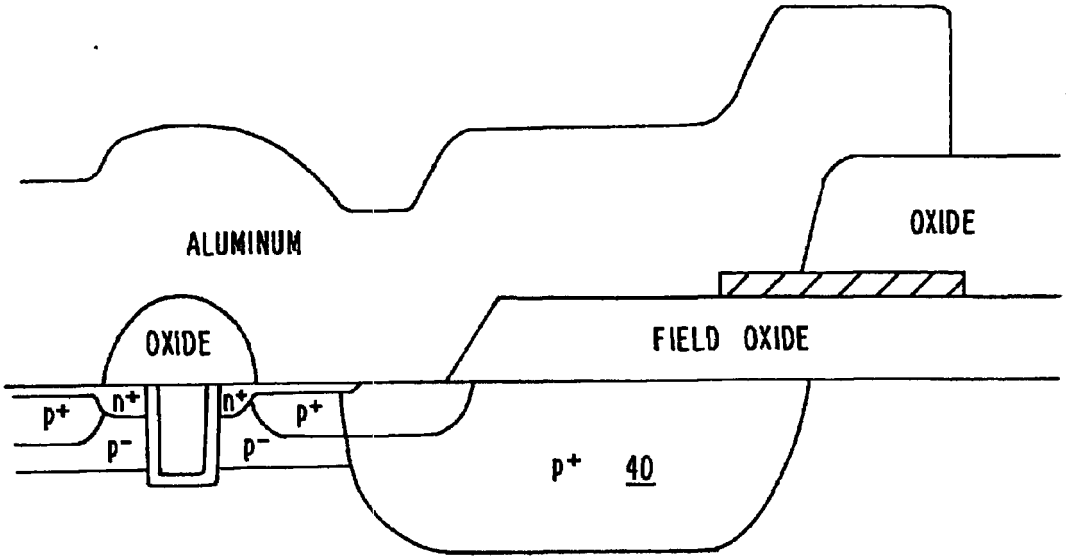


FIG. 2.

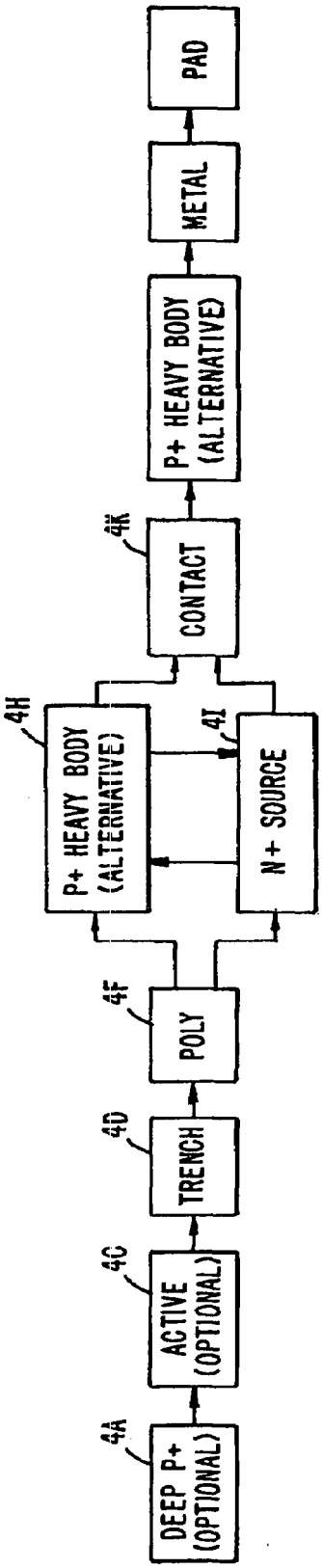

PAD
METAL
P+ HEAVY BODY (ALTERNATIVE)
4K
CONTACT
4H
P+ HEAVY BODY (ALTERNATIVE)
4I
N+ SOURCE
4F
POLY
4D
TRENCH
4C
ACTIVE (OPTIONAL)
4A
DEEP P+ (OPTIONAL)

FIG. 3.

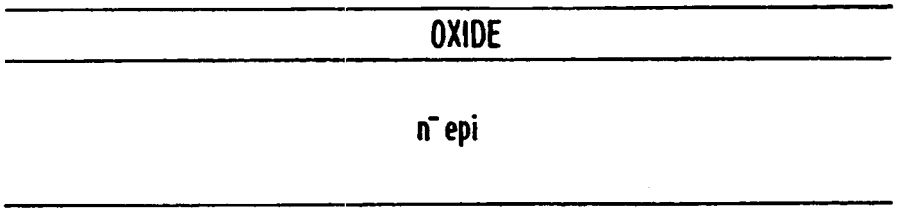


FIG. 4.

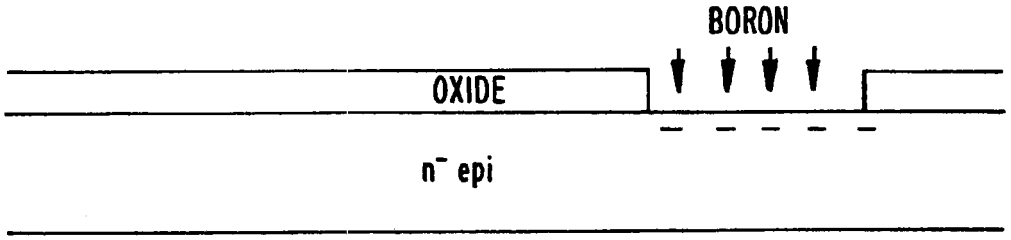


FIG. 4A.

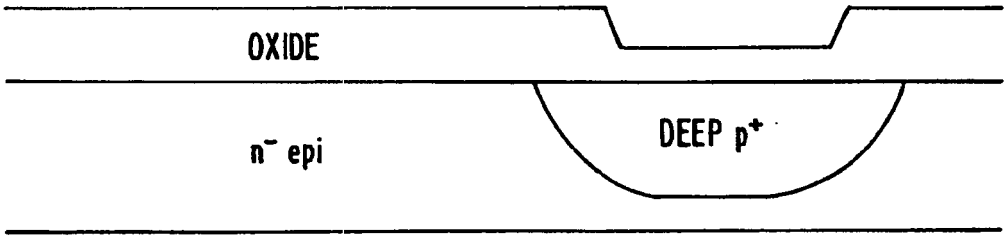


FIG. 4B.

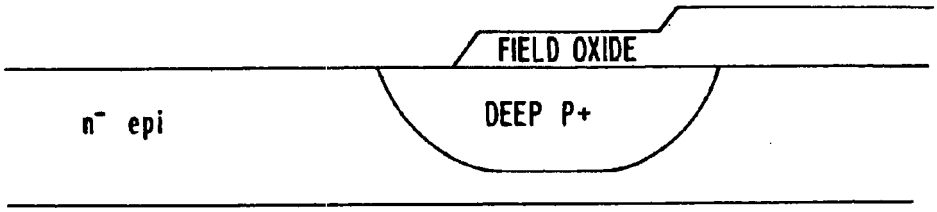


FIG. 4C.

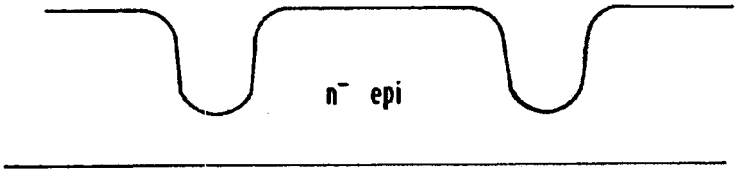


FIG. 4D.

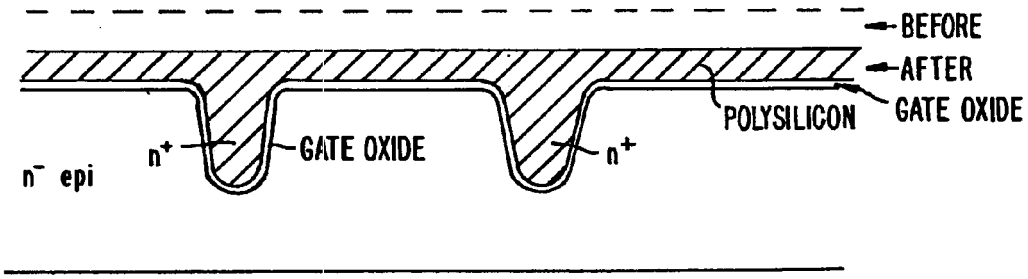


FIG. 4E.

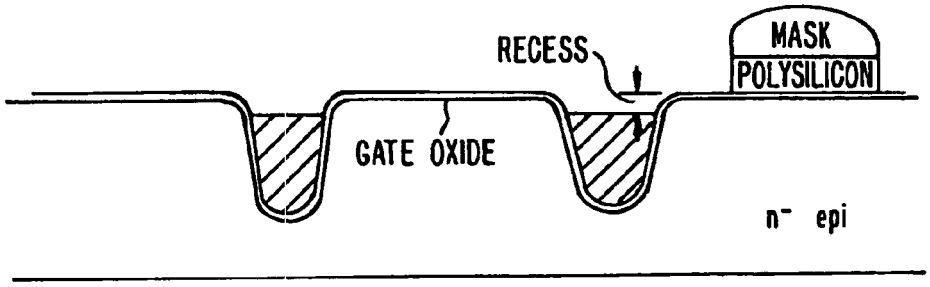


FIG. 4F.

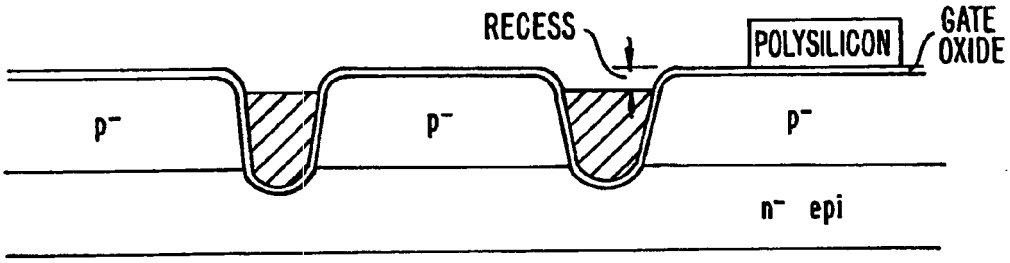


FIG. 4G.

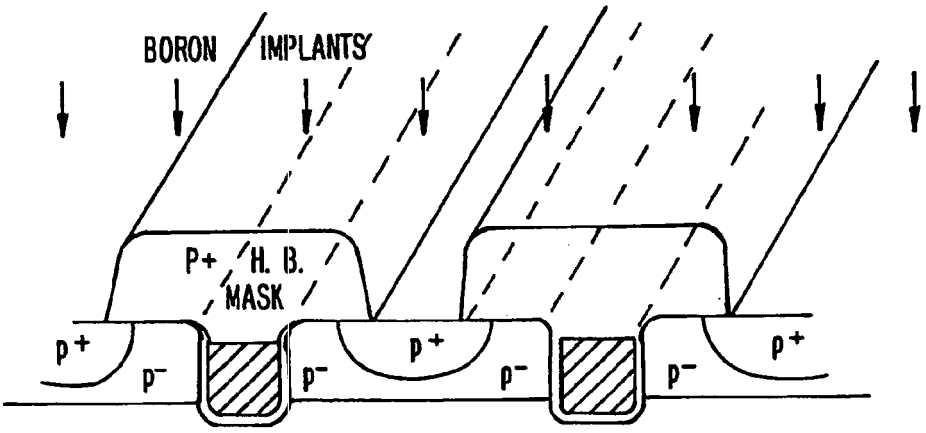


FIG. 4H.

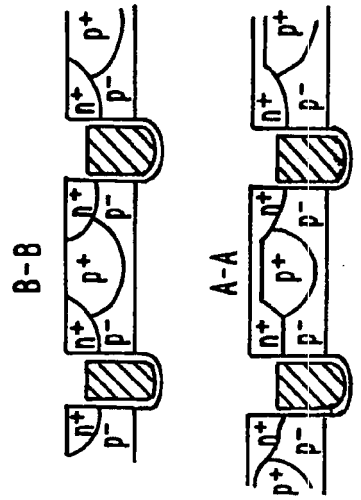


FIG. 4I.

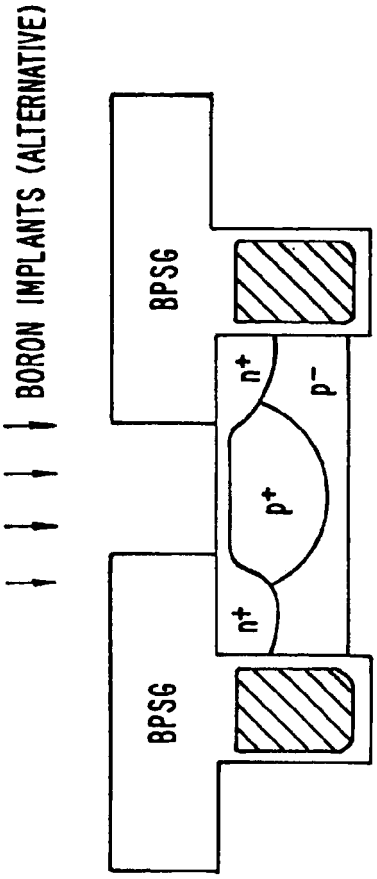
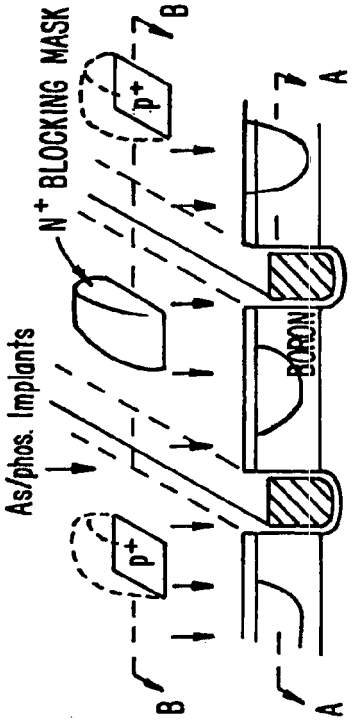


FIG. 4K.



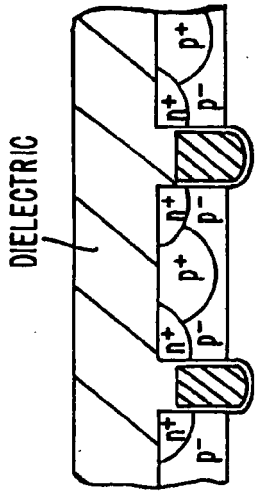


FIG. 4J.

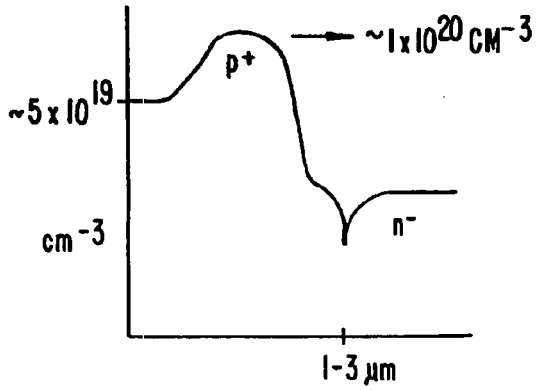


FIG. 5.

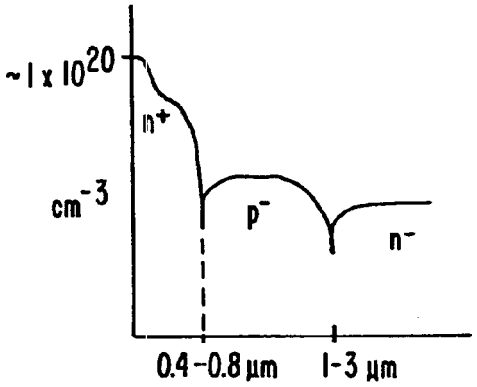


FIG. 5A.

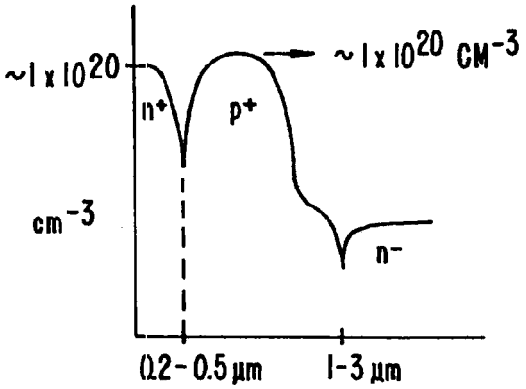


FIG. 5B.

METHOD OF MANUFACTURING A TRENCH TRANSISTOR HAVING A HEAVY BODY REGION

This application is a continuation of and claims the benefit of U.S. application Ser. No. 10/347,254, filed Jan. 17, 2003, now U.S. Pat. No. 6,828,195, which is a continuation of U.S. application Ser. No. 09/854,102 filed May 9, 2001, now U.S. Pat. No. 6,521,497, which is a divisional of U.S. application Ser. No. 08/970,221 filed Nov. 14, 1997, now U.S. Pat. No. 6,429,481.

BACKGROUND OF THE INVENTION

The present invention relates to field effect transistors, in particular trench DMOS transistors, and methods of their manufacture.

Power field effect transistors, e.g., MOSFETs (metal oxide semiconductor field effect transistors), are well known in the semiconductor industry. One type of MOSFET is a DMOS (double diffused metal oxide semiconductor) transistor. DMOS transistors typically include a substrate on which an epitaxial layer is grown, a doped source junction, a doped heavy body, a doped well of the same (p or n) doping as the heavy body, and a gate electrode. In trenched DMOS transistors the gate electrode is a vertical trench. The heavy body is typically diffused deeper than the bottom of the trench, to minimize electric field at the bottom corners of the trench and thereby prevent avalanche breakdown from damaging the device. The trench is filled with conductive polysilicon, and the polysilicon is generally overetched, to assure that it is completely removed from the surface surrounding the trench. This overetching generally leaves a recess between the top of the polysilicon and the surface of the semiconductor substrate (i.e., the surface of the epitaxial layer). The depth of this recess must be carefully controlled so that it is shallower than the depth of the source junctions. If the recess is deeper than the source junctions the source may miss the gate, resulting in high on-state resistance, high threshold, and potentially a non-functional transistor.

The source and drain junctions can be doped with either p-type or n-type dopants; in either case, the body will be doped with the opposite dopant, e.g., for n-type source and drain the body will be p-type. DMOS transistors in which the source and drain are doped with p-type carriers are referred to as "p-channel". In p-channel DMOS transistors a negative voltage applied to the transistor gate causes current flow from the source region, through a channel region of the body, an accumulation region of the epitaxial layer, and the substrate, to the drain region. Conversely, DMOS transistors, in which the source and drain are doped with n-type carriers, are referred to as "n-channel". In n-channel DMOS transistors a positive voltage applied to the transistor gate causes current to flow from drain to source.

It is desirable that DMOS transistors have low source to drain resistance (Rds_{on}) when turned on and low parasitic capacitance. The transistor structure should also avoid "punchthrough". Punchthrough occurs when, upon application of a high drain to source voltage, depletion into the body region extends to the source region, forming an undesirable conductive path through the body region when the transistor should be off. Finally, the transistor should have good "ruggedness", i.e., a high activation current is needed to turn on the parasitic transistor that inherently exists in DMOS transistors.

Generally a large number of MOSFET cells are connected in parallel forming a single transistor. The cells may be arranged in a "closed cell" configuration, in which the trenches are laid out in a grid pattern and the cells are enclosed on all sides by trench walls. Alternatively, the cells may be arranged in an "open cell" configuration, in which the trenches are laid out in a "stripe" pattern and the cells are only enclosed on two sides by trench walls. Electric field termination techniques are used to terminate junctions (doped regions) at the periphery (edges) of the silicon die on which the transistors are formed. This tends to cause the breakdown voltage to be higher than it would otherwise be if controlled only by the features of the active transistor cells in the central portions of the die.

SUMMARY OF THE INVENTION

The present invention provides field effect transistors that have an open cell layout that provides good uniformity and high cell density and that is readily scalable. Preferred trenched DMOS transistors exhibit low Rds_{on}, low parasitic capacitance, excellent reliability, resistance to avalanche breakdown degradation, and ruggedness. Preferred devices also include a field termination that enhances resistance to avalanche breakdown. The invention also features a method of making trench DMOS transistors.

In one aspect, the invention features a trenched field effect transistor that includes (a) a semiconductor substrate, (b) a trench extending a predetermined depth into the semiconductor substrate, (c) a pair of doped source junctions, positioned on opposite sides of the trench, (d) a doped heavy body positioned adjacent each source junction on the opposite side of the source junction from the trench, the deepest portion of the heavy body extending less deeply into said semiconductor substrate than the predetermined depth of the trench, and (e) a doped well surrounding the heavy body beneath the heavy body.

Preferred embodiments include one or more of the following features. The doped well has a substantially flat bottom. The depth of the heavy body region relative to the depths of the well and the trench is selected so that the peak electric field, when voltage is applied to the transistor, will be spaced from the trench. The doped well has a depth less than the predetermined depth of the trench. The trench has rounded top and bottom corners. There is an abrupt junction at the interface between the heavy body and the well, to cause the peak electric field, when voltage is applied to the transistor, to occur in the area of the interface.

In another aspect, the invention features an array of transistor cells. The array includes (a) a semiconductor substrate, (b) a plurality of gate-forming trenches arranged substantially parallel to each other and extending in a first direction, the space between adjacent trenches defining a contact area, each trench extending a predetermined depth into said substrate, the predetermined depth being substantially the same for all of said gate-forming trenches; (c) surrounding each trench, a pair of doped source junctions, positioned on opposite sides of the trench and extending along the length of the trench, (d) positioned between each pair of gate-forming trenches, a doped heavy body positioned adjacent each source junction, the deepest portion of each said heavy body extending less deeply into said semiconductor substrate than said predetermined depth of said trenches, (e) a doped well surrounding each heavy body beneath the heavy body; and (f) p+ and n+ contacts disposed at the surface of the semiconductor substrate and arranged in alternation along the length of the contact area.

Preferred embodiments include one or more of the following features. The first and second dopants both comprise

boron. The first energy is from about 150 to 200 keV. The first dosage is from about 1E15 to 5E15 cm^{-2}. The second energy is from about 20 to 40 keV. The second dosage is from about 1E14 to 1E15 cm^{-2}.

In yet another aspect, the invention features a semiconductor die that includes (a) a plurality of DMOS transistor cells arranged in an array on a semiconductor substrate, each DMOS transistor cell including a gate-forming trench, each of said gate-forming trenches having a predetermined depth, the depth of all of the gate-forming trenches being substantially the same; and (b) surrounding the periphery of the array, a field termination structure that extends into the semiconductor substrate to a depth that is deeper than said predetermined depth of said gate-forming trenches.

Preferred embodiments include one or more of the following features. The field termination structure includes a doped well. The field termination structure includes a termination trench. The field termination structure includes a plurality of concentrically arranged termination trenches. Each of the DMOS transistor cells further comprises a doped heavy body and the doped heavy body extends into the semiconductor substrate to a depth than is less than the predetermined depth of the gate-forming trenches.

The invention also features a method of making a heavy body structure for a trenched DMOS transistor including (a) providing a semiconductor substrate; (b) implanting into a region of the substrate a first dopant at a first energy and dosage; and (c) subsequently implanting into said region a second dopant at a second energy and dosage, said second energy and dosage being relatively less than said first energy and dosage.

Preferred embodiments include one or more of the following features. The first and second dopants both comprise boron. The first energy is from about 150 to 200 keV. The first dosage is from about 1E15 to 5E15. The second energy is from about 20 to 40 keV. The second dosage is from about 1E14 to 1E15.

Additionally, the invention features a method of making a source for a trenched DMOS transistor including (a) providing a semiconductor substrate; (b) implanting into a region of the substrate a first dopant at a first energy and dosage; and (c) subsequently implanting into the region a second dopant at a second energy and dosage, the second energy and dosage being relatively less than the first energy and dosage.

Preferred embodiments include one or more of the following features. The first dopant comprises arsenic and the second dopant comprises phosphorus. The first energy is from about 80 to 120 keV. The first dosage is from about 5E15 to 1E16 cm^{-2}. The second energy is from about 40 to 70 keV. The second dosage is from about 1E15 to 5E15 cm^{-2}. The resulting depth of the source is from about 0.4 to 0.8 m the finished DMOS transistor.

In another aspect, the invention features a method of manufacturing a trenched field effect transistor. The method includes (a) forming a field termination junction around the perimeter of a semiconductor substrate, (b) forming an epitaxial layer on the semiconductor substrate, (c) patterning and etching a plurality of trenches into the epitaxial layer; (d) depositing polysilicon to fill the trenches, (e) doping the polysilicon with a dopant of a first type, (f) patterning the substrate and implanting a dopant of a second, opposite type to form a plurality of wells interposed between adjacent trenches, (g) patterning the substrate and implanting a dopant of the second type to form a plurality of second dopant type contact areas and a plurality of heavy bodies positioned above the wells, each heavy body having an abrupt junction with the corresponding well, (h) patterning the substrate and implanting a dopant of the first type to provide source regions and first dopant type contact areas; and (i) applying a dielectric to the surface of the semiconductor substrate and patterning the dielectric to expose electrical contact areas.

Other features and advantages of the invention will be apparent from the following detailed description, and from the claims.

BRIEF DESCRIPTION OF THE DRAWINGS

FIG. **1** is a highly enlarged, schematic perspective cross-sectional view showing a portion of a cell array including a plurality of DMOS transistors according to one aspect of the invention. The source metal layer and a portion of the dielectric layer have been omitted to show the underlying layers. FIGS. **1***a* and **1***b* are side cross-sectional views of a single line of transistors from the array of FIG. **1**, taken along lines A—A and B—B, respectively. In FIGS. **1***a* and **1***b* the source metal and dielectric layers are shown.

FIG. **2** is a highly enlarged schematic side cross-sectional view of a semiconductor die showing a portion of the cell array and the field termination.

FIG. **3** is a flow diagram showing the photo mask sequence of a preferred process for forming a trench DMOS transistor of FIG. **1**.

FIGS. **4**–**4**K are schematic side cross-sectional views showing the individual steps of the process diagrammed in FIG. **3**. The figure numbers for the detailed views in FIGS. **4**–**4**K are shown parenthetically under the corresponding diagram boxes in FIG. **3**.

FIGS. **5**, **5**A, and **5**B are spreading resistance profile graphs, reflecting the dopant concentration distribution at different regions of the transistor.

DESCRIPTION OF THE PREFERRED EMBODIMENTS

A cell array **10**, including a plurality of rows **12** of trenched DMOS transistors, is shown in FIG. **1**. Cell array **10** has an open cell configuration, i.e., trenches **14** run in only one direction, rather than forming a grid. Individual cells are formed by alternating n+ source contacts **16** and p+ contacts **18** in rows **20** that run parallel to and between trenches **14**. The configuration of the regions of each row that have an n+ source contact are shown in cross-section in FIG. **1**A, while the regions that have a p+ contact are shown in FIG. **1**B.

As shown in FIGS. **1**A and **1**B, each trenched DMOS transistor includes a doped n+ substrate (drain) layer **22**, a more lightly doped n− epitaxial layer **24**, and a gate electrode **28**. Gate electrode **28** comprises a conductive polysilicon that fills a trench **14**. A gate oxide **26** coats the walls of the trench and underlies the polysilicon. The top surface of the polysilicon is recessed from the surface **30** of the semiconductor substrate by a distance R (typically from about 0 to 0.4 m). N+ doped source regions **32***a*, **32***b* are positioned one on each side of the trench **14**. A dielectric layer **35** covers the trench opening and the two source regions **32***a*, **32***b*. Extending between the source regions of adjacent cells is a p+ heavy body region **34** and, beneath it, a flat-bottomed p− well **36**. In the areas of the cell array which have a n+ contact **16**, a shallow n+ doped contact region extends between the n+ source regions. A source metal layer **38** covers the surface of the cell array.

The transistor shown in FIGS. **1**A and **1**B includes several features that enhance the ruggedness of the transistor and its resistance to avalanche breakdown degradation.

First, the depth of the p+ heavy body region **34** relative to the depths of the trench **14** and the flat bottom of the p− well is selected so that the peak electric field when voltage is applied to the transistor will be approximately halfway between adjacent trenches. The preferred relative depths of the p+ heavy body, the p− well and the trench are different for different device layouts. However, preferred relative depths can be readily determined empirically (by observing the location of peak electric field) or by finite element analysis.

Second, the bottom corners of the trench **14** are rounded (preferably, the top corners are also rounded; this feature is not shown). Comer rounding can be achieved using the process described in U.S. application Ser. No. 08/959,197, filed on Oct. 28, 1997, now U.S. Pat. No. 6,103,635. The rounded corners of the trench also tend to cause the peak electric field to be moved away from the trench corners and towards a central location between adjacent trenches.

Third, an abrupt junction at the interface between the p+ heavy body and the p-well causes the peak electric field to occur in that area of the interface. Avalanche multiplication initiates at the location of the peak electric field, thus steering hot carriers away from the sensitive gate oxide and channel regions. As a result, this structure improves reliability and avalanche ruggedness without sacrificing cell density as much as a deeper heavy body junction. This abrupt junction can be achieved by the double doping process that will be described below, or by other processes for forming abrupt junctions, many of which are known in the semiconductor field.

Lastly, referring to FIG. **2**, the cell array is surrounded by a field termination junction **40** which increases the breakdown voltage of the device and thaws avalanche current away from the cell array to the periphery of the die. Field termination junction **40** is a deep p+ well, preferably from about 1 to 3 m deep at its deepest point, that is deeper than the p+ heavy body regions **34** in order to reduce the electric field caused by the junction curvature. A preferred process for making the above-described transistors is shown as a flow diagram in FIG. **3**, and the individual steps are shown schematically in FIGS. **4**–**4**K. It is noted that some steps that are conventional or do not require illustration are described below but not shown in FIGS. **4**–**4**K. As indicated by the arrows in FIG. **3**, and as will be discussed below, the order of the steps shown in FIGS. **4**–**4**K can be varied. Moreover, some of the steps shown in FIGS. **4**–**4**K are optional, as will be discussed.

A semiconductor substrate is initially provided. Preferably, the substrate is a N++ Si substrate, having a standard thickness, e.g., 500 μm, and a very low resistivity, e.g., 0.001 to 0.005 Ohm-cm. An epitaxial layer is deposited onto this substrate, as is well known, preferably to a thickness of from about 4 to 10 μm. Preferably the resistivity of the epitaxial layer is from about 0.1 to 3.0 Ohm-cm.

Next, the field termination junction **40** is formed by the steps shown in FIGS. **4**–**4**C. In FIG. **4**, an oxide layer is formed on the surface of the epitaxial layer. Preferably, the thickness of the oxide is from about 5 to 10 kÅ. Next, as shown in FIG. **4**A, the oxide layer is patterned and etched to define a mask, and the p+ dopant is introduced to form the deep p+ well field termination. A suitable dopant is boron, implanted at an energy of from about 40 to 100 keV and a dose of 1E14 (1×10^{14}) to 1E16 cm^{-2}. As shown in FIG. **4**B, the p+ dopant is then driven further into the substrate, e.g., by diffusion, and a field oxide layer is formed over the p+ junction. Preferably the oxide thickness is from about 4 to 10 kÅ. Finally, the oxide (FIG. **4**) over the active area of the substrate (the area where the cell array will be formed) is patterned and removed by any suitable etching process, leaving only the field oxide in suitable areas. This leaves the substrate ready for the following steps that will form the cell array.

It is noted that, as an alternative to steps **4**–**4**C, a suitable field termination structure can be formed using a ring-shaped trench which surrounds the periphery of the cell array and acts to lessen the electric field and increase the resistance to avalanche breakdown degradation. This trench field termination does not require a field oxide or deep p+ body junction to be effective. Consequently, it can be used to reduce the number of process steps. Using a trench ring (or multiple concentric trench rings) to form a field termination is described in, e.g., U.S. Pat. No. 5,430,324, the full disclosure of which is hereby incorporated herein by reference. Preferably, the trench would have substantially the same depth as the trenches in the cell array.

The cell array is formed by the steps shown in FIGS. **4**D–**4**K. First, a plurality of trenches are patterned and etched into the epitaxial layer of the substrate (FIG. **4**D). Preferably, as noted above, the trenches are formed using the process described in U.S. application Ser. No. 08/959,197, filed on Oct. 28, 1997, now U.S. Pat. No. 6,103,635, so that the upper and lower corners of each trench will be smoothly rounded. As shown in FIG. **1** and described above, the trenches are patterned to run in only one direction, defined as an open cell structure. After trench formation, a gate oxide layer is formed on the trench walls, as is well known in the semiconductor field. Preferably the gate oxide has a thickness of from about 100 to 800 Å.

Next, as shown in FIG. **4**E, polysilicon is deposited to fill the trench and cover the surface of the substrate, generally to a thickness of from about 1 to 2 m depending on the trench width (shown by the dotted lines in FIG. **4**E). This layer is then planarized by the nature of its thickness relative to the trench width, typically from about 2 to 5 k Å (indicated by solid lines in FIG. **4**E). The polysilicon is then doped to n-type, e.g., by conventional $POCL_3$ doping or by phosphorus implant. The backside of the wafer need not be stripped (as is conventionally done prior to doping the polysilicon to enhance defect gettering) because any further doping of the highly doped substrate would be unlikely to result in any enhancement in defect gettering.

The polysilicon is then patterned with a photoresist mask and etched to remove it from the trench areas, as shown in FIG. **4**F. A small recess between the top of the polysilicon in the trench and the substrate surface inherently results when the polysilicon is etched completely to remove all of the polysilicon from the substrate surface. The depth of this recess must be controlled so that it does not exceed the depth of the n+ source junction that will be formed in a later step. To reduce the need to carefully control this aspect of the process, a relatively deep n+ source junction is formed, as will be discussed below.

Then, as shown in FIG. **4**G, the p-well is formed by implanting the dopant, e.g., a boron implant at an energy of 30 to 100 keV and a dosage of 1E13 to 1E15, and driving it in to a depth of from about 1 to 3 m using conventional drive in techniques.

The next two steps (p+ heavy body formation) can be performed either before formation of the n+ source junction, or afterwards, as indicated by the arrows in FIG. **3**. P+ heavy body formation and n+ source junction formation can be

performed in either order because they are both resist-masked steps and because there is no diffusion step in between. This advantageously allows significant process flexibility. The p+ heavy body formation steps will be described below as being performed prior to source formation; it will be understood that n+ source formation could be performed first simply by changing the order of the steps discussed below.

First, a mask is formed over the areas that will not be doped to p+, as shown in FIG. **4**H. (It is noted that this masking step is not required if the p+ heavy body is formed later, after the dielectric layer has been applied and patterned for contact holes. (see FIG. **4**K, below) so that the dielectric itself provides a mask.) As discussed above, it is preferred that the junction at the interface between the p− well and the p+ heavy body be abrupt. To accomplish this, a double implant of dopant (e.g., boron) is performed. For example, a preferred double implant is a first boron implant at an energy of 150 to 200 keV and a dose of 1E15 to 5E15 cm^{-2}, and a second boron implant at an energy of 20 to 40 keV and a dose of 1E14 to 1E15 cm^{-2}. The high energy first implant brings the p+ heavy body as deep as possible into the substrate, so that it will not compensate the n+ source junction to be introduced later. The second, lower energy/lower dose implant extends the p+ heavy body from the deep region formed during the first implant up to the substrate surface to provide the p+ contact **18**. The resulting p+ heavy body junction is preferably about 0.4 to 1 m deep at this stage of the process (final junction depth after drive-in is preferably about 0.5 to 1.5 m deep), and includes a region of high dopant concentration near the interface with the p-well, and a region of relatively low dopant concentration at the contact surface of the p+ heavy body. A preferred concentration distribution is shown in FIG. **5**.

It will be appreciated by those skilled in the art that the abrupt junction can be formed in many other ways, e.g., by diffused dopants, by using a continuous dopant source at the surface or by using atoms that diffuse slowly.

After the formation of the p+ heavy body, a conventional resist strip process is performed to remove the mask, and a new mask is patterned to prepare the substrate for the formation of the n+ source junction. This mask is a n+ blocking mask and is patterned to cover the areas of the substrate surface which are to provide p+ contacts **18** (FIGS. **1** and 1B), as shown in FIG. **4**I. This results in the formation of alternating p+ and n+ contacts after n-type doping (see lines A—A and B—B and cross-sectional views A—A and B—B in FIG. 4I, which correspond to FIGS. 1A and **1**B).

The n+ source regions and n+ contact are then formed using a double implant. For example, a preferred double implant process -is a first implant of arsenic at an energy of 80 to 120 keV and a dose of 5E15 to 1E16 cm^{-2} followed by a second implant of phosphorus at an energy of 40 to 70 keV and a dose of 1E15 to 5E15 cm^{-2}. The phosphorus implant forms a relatively deep n+ source junction, which allows more process flexibility in the depth of the polysilicon recess, as discussed above. Phosphorus ions will penetrate deeper into the substrate during implant and also during later diffusion steps. Advantageously, the n+ source regions will have a depth of about 0.4 to 0.8 m after diffusion. The arsenic implant extends the n+ source to the substrate surface, and also forms the n contacts **16** (see FIGS. **1** and 1A) by compensating (converting) the p-type surface of the p+ heavy body to n-type in the desired contact area. The preferred sheet resistance profiles for the n+ source along the edge of the trench, and the n+ contact are shown in FIGS. **5**A and **5**B respectively.

Thus, the alternating p+ and n+ contacts **18**, **16**, shown in FIG. **1** are formed by patterning the substrate with appropriate masks and doping with the first p+ implant and the second n+ implant, respectively, as described above. This manner of forming the alternating contacts advantageously allows an open cell array having a smaller cell pitch than is typical for such arrays and thus a higher cell density and lower Rds_{on}.

Next, a conventional n+ drive is performed to activate the dopants. A short cycle is used, preferably 10 min at 900° C., so that activation occurs without excessive diffusion.

A dielectric material, e.g., borophosphate silicate glass (BPSG), is then deposited over the entire substrate surface and flowed in a conventional manner (FIG. **4**J), after which the dielectric is patterned and etched (FIG. **4**K) to define electrical contact openings over the n+ and p+ contacts **16**, **18**.

As noted above, the p+ heavy body implant steps can be performed at this point, if desired (rather than prior to n+ source formation), eliminating the need for a mask and thus reducing cost and process time.

Next, the dielectric is reflowed in an inert gas, e.g., a nitrogen purge. If the p+ body has been implanted immediately prior, this step is required to activate the p+ dopant. If the p+ body was implanted earlier, prior to the n+ drive, this step can be omitted if the dielectric surface is sufficiently smooth-edged around the contact openings.

The cell array is then completed by conventional metalization, passivation deposition and alloy steps, as is well known in the semiconductor field.

Other embodiments are within the claims. For example, while the description above is of an n-channel transistor, the processes of the invention could also be used to form a p-channel transistor. To accomplish this, "p" and "n" would simply be reversed in the above description, i.e., where "p" doping is specified above the region would be "if" doped instead, and vice versa.

The invention claimed is:

1. A method of manufacturing a trench transistor comprising:

providing a semiconductor substrate having dopants of a first conductivity type;

forming a plurality of trenches extending from a first surface of the substrate to a first depth into the semiconductor substrate;

lining each of the plurality of trenches with a gate dielectric material;

substantially filling each dielectric-lined trench with conductive material;

forming a doped well in the substrate to a second depth that is less than said first depth of the plurality of trenches, the doped well having dopants of a second conductivity type opposite to said first conductivity type;

forming a source region inside the doped well and extending to a third depth that is less than the second depth, the source region having dopants of the first conductivity type; and

forming a heavy body inside the doped well, the heavy body having dopants of the second conductivity type with a peak concentration occurring at a fourth depth below the third depth of the source region and above the second depth of the doped well.

2. The method of claim **1** wherein the step of forming a doped well forms the well with a substantially flat bottom.

3. The method of claim **1** further comprising forming a deep doped region having dopants of the second conductivity type, the deep doped region extending into the substrate to a fourth depth that is deeper than said first depth of the trench.

4. The method of claim 3 wherein the step of forming a deep doped region forms a PN junction diode with the substrate that helps improve a breakdown voltage of the transistor.

5. The method of claim 3 wherein the deep doped region forms a termination structure around the periphery of the substrate.

6. The method of claim 1 wherein the step of substantially filling each dielectric-lined trench leaves a recess at an upper portion of each trench.

7. The method of claim 6 further comprising filling the recess at the upper portion of each trench with dielectric material.

8. The method of claim 1 wherein the step of forming the heavy body comprises a double implant process.

9. The method of claim 8 wherein the double implant process comprises:

a first implant of dopants of the first conductivity type, at a first energy level and a first dosage to form a first doped portion of the heavy body; and

a second implant of dopants of the first conductivity type, at a second energy level and a second dosage to form a second doped portion of the heavy body.

10. The method of claim 9 wherein the first implant occurs at approximately the fourth depth.

11. The method of claim 9 wherein the first energy level is higher than the second energy level.

12. The method of claim 11 wherein the first dosage is higher than the second dosage.

13. The method of claim 1 wherein the step of forming the heavy body comprises a process of diffusing dopants of the second conductivity type.

14. The method of claim 1 wherein the step of forming the heavy body comprises using a continuous dopant source at the surface of the semiconductor substrate.

15. The method of claim 1 wherein the step of forming a plurality of trenches comprises patterning and etching the plurality of trenches that extend in parallel along a longitudinal axis.

16. The method of claim 15 further comprising forming a contact area on the surface of the substrate between adjacent trenches.

17. The method of claim 16 wherein the step of forming the contact area comprises forming alternating source contact regions and heavy body contact regions.

18. The method of claim 16 wherein the step of forming the contact area comprises forming a ladder-shaped source contact region surrounding heavy body contact regions.

19. The method of claim 18 wherein the step of forming the ladder-shaped source contact region surrounding heavy body contact regions, comprises:

forming a source blocking mask on the surface of the semiconductor substrate patterned to cover the heavy body contact regions; and

implanting dopants of the first conductivity type to form the ladder-shaped source contact region.

20. The method of claim 18 wherein the step of forming the ladder-shaped source contact region surrounding heavy body contact regions, comprises forming a dielectric layer on the surface of the semiconductor substrate patterned to expose the heavy body contact regions.

21. The method of claim 1 wherein the source region is formed prior to the heavy body.

22. The method of claim 1 wherein the step of providing a semiconductor substrate comprises:

forming a drain contact region at a second surface opposite to the first surface of the substrate; and

forming a substantially uniformly doped epitaxial layer atop said drain contact region.

23. A method of manufacturing a trench transistor comprising:

providing a semiconductor substrate having dopants of a first conductivity type;

forming a plurality of trenches extending from a first surface of the substrate to a first depth into the semiconductor substrate;

lining each of the plurality of trenches with a gate dielectric material;

substantially filling each dielectric-lined trench with conductive material;

forming a doped well in the substrate to a second depth that is less than said first depth of the plurality of trenches, the doped well having dopants of a second conductivity type opposite to said first conductivity type;

forming a source region inside the doped well to a third depth, the source region having dopants of the first conductivity type; and

forming a heavy body inside the doped well to a fourth depth between the third depth of the source region and the second depth of the doped well, the heavy body having dopants of the second conductivity type with a dopant concentration that is higher near the interface with the doped well than near the first surface.

24. The method of claim 23 further comprising forming a deep doped region having dopants of the second conductivity type, the deep doped region extending into the substrate to a fifth depth that is deeper than said first depth of the trench.

25. The method of claim 24 wherein the step of forming a deep doped region forms a PN junction diode with the substrate that helps improve a breakdown voltage of the transistor.

26. The method of claim 24 wherein the deep doped region forms a termination structure around the periphery of the substrate.

27. The method of claim 23 wherein the source region is formed prior to the heavy body.

28. The method of claim 23 wherein the step of providing a semiconductor substrate comprises:

forming a drain contact region at a second surface opposite to the first surface of the substrate; and

forming a substantially uniformly doped epitaxial layer atop said drain contact region.

29. A method of manufacturing a trench transistor comprising:

providing a semiconductor substrate having dopants of a first conductivity type, the semiconductor substrate including a first highly doped drain layer and a second more lightly and substantially uniformly doped epitaxial layer atop and adjacent the first layer;

forming a plurality of trenches extending to a first depth into the epitaxial layer, the plurality of trenches creating a respective plurality of epitaxial mesas;

lining each of the plurality of trenches with a gate dielectric material;

substantially filling each dielectric-lined trench with conductive material;

forming a plurality of doped wells in the plurality of epitaxial mesas, respectively to a second depth that is less than said first depth of the plurality of trenches, the plurality of doped wells having dopants of a second conductivity type opposite to said first conductivity type;

forming a plurality of source regions adjacent the plurality of trenches and inside the plurality of doped wells, the source regions having a third depth and dopants of the first conductivity type;

forming a plurality of heavy body regions each inside a respective one of the plurality of doped wells, each heavy body region having a fourth depth between the third depth of the source region and the second depth of the doped well, and having dopants of the second conductivity type; and

adjusting a dopant profile of the plurality of heavy body regions so that peak electric field is moved away from a nearby trench toward the heavy body resulting in avalanche current that is substantially uniformly distributed.

30. The method of claim **29** wherein the step of forming the plurality of heavy body regions comprises a double implant process.

31. The method of claim **30** wherein the double implant process comprises:

a first implant of dopants of the first conductivity type, at a first energy level and a first dosage to form a first doped portion of the heavy body; and

a second implant of dopants of the first conductivity type, at a second energy level and a second dosage to form a second doped portion of the heavy body.

32. The method of claim **31** wherein the first implant occurs at approximately the fourth depth.

33. The method of claim **31** wherein the first energy level is higher than the second energy level.

34. The method of claim **33** wherein the first dosage is higher than the second dosage.

35. The method of claim **29** wherein the step of forming the plurality of heavy body regions comprises a process of diffusing dopants of the second conductivity type.

36. The method of claim **29** wherein the step of forming the plurality of heavy body regions comprises using a continuous dopant source at the surface of the semiconductor substrate.

* * * * *

UNITED STATES PATENT AND TRADEMARK OFFICE

CERTIFICATE OF CORRECTION

PATENT NO. : 7,148,111 B2
APPLICATION NO. : 10/927788
DATED : December 12, 2006
INVENTOR(S) : Brian Sze-Ki Mo et al.

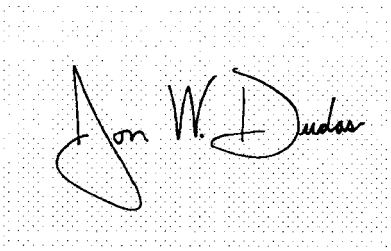
It is certified that error appears in the above-identified patent and that said Letters Patent is hereby corrected as shown below:

Title Page
In the Assignee information (73):

"San Jose, CA" should be --South Portland, ME--.

Signed and Sealed this

Sixth Day of March, 2007



JON W. DUDAS
Director of the United States Patent and Trademark Office

EXHIBIT BB

US006818947B2

(12) **United States Patent**
Grebs et al.

(10) **Patent No.: US 6,818,947 B2**
(45) **Date of Patent: Nov. 16, 2004**

(54) **BURIED GATE-FIELD TERMINATION STRUCTURE**

(75) Inventors: **Thomas E. Grebs**, Mountaintop, PA (US); **Christopher B. Kocon**, Plains, PA (US); **Rodney S. Ridley, Sr.**, Mountaintop, PA (US); **Gary M. Dolny**, Mountaintop, PA (US); **Nathan Lawrence Kraft**, Wilkes-Barre, PA (US); **Louise E. Skurkey**, Conyngham, PA (US)

(73) Assignee: **Fairchild Semiconductor Corporation**, South Portland, ME (US)

(*) Notice: Subject to any disclaimer, the term of this patent is extended or adjusted under 35 U.S.C. 154(b) by 0 days.

(21) Appl. No.: **10/247,464**

(22) Filed: **Sep. 19, 2002**

(65) **Prior Publication Data**

US 2004/0056302 A1 Mar. 25, 2004

(51) **Int. Cl.**[7] **H01L 29/76**

(52) **U.S. Cl.** **257/330**; 257/329; 257/331; 257/332; 438/259; 438/270; 438/271; 438/589

(58) **Field of Search** 257/302–339

(56) **References Cited**

U.S. PATENT DOCUMENTS

4,876,579	A	10/1989	Davis et al.
5,233,215	A	8/1993	Baliga
5,578,851	A	11/1996	Hshieh et al.
5,605,852	A	2/1997	Bencuya
5,639,676	A	6/1997	Hshieh et al.
6,110,763	A	8/2000	Temple
6,188,105	B1	2/2001	Kocon et al.
6,362,026	B2	3/2002	Zeng et al.

OTHER PUBLICATIONS

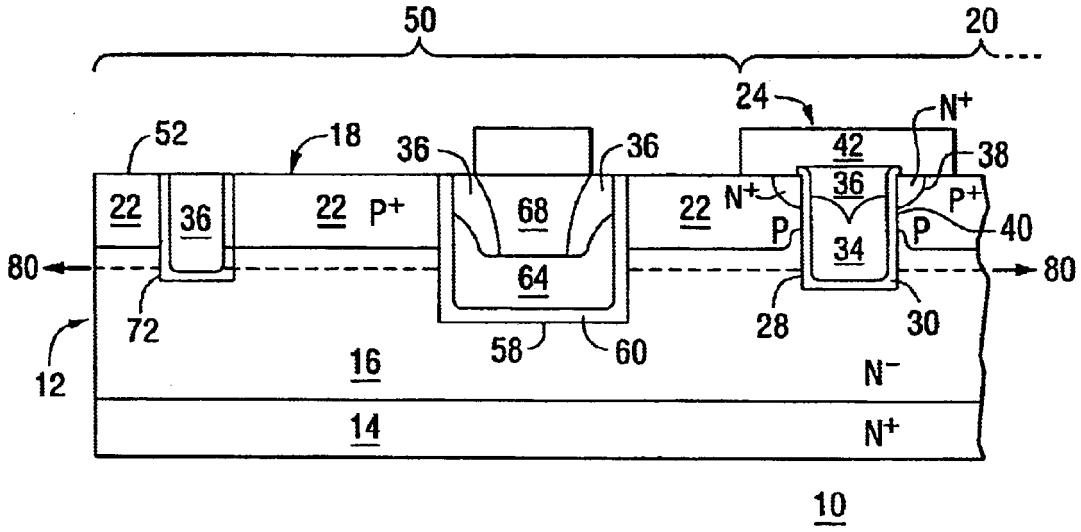
B. Jayant Baliga, Power Semiconductor Devices, Chapter 3: Breakdown Voltage; Section 3.6, Edge Terminations, pp. 81–112, PWS Publishing Company, Boston, MA, Copyright 1996.

Primary Examiner—Fetsum Abraham
(74) *Attorney, Agent, or Firm*—Laurence S. Roach, Esq.; Law Office of Thomas R. FitzGerald

(57) **ABSTRACT**

In a power semiconductor device **10**, a continuous trench has an outer circumferential portion **58** that includes a field plate and inner portions **28** that carry include one or more gate runners **34** to that the gate runners and the field plate are integral with each other. The trench structure **58**, **28** is simpler to form and takes up less surface space that the separate structures of the prior art. The trench is lined with an insulator and further filled with conductive polysilicon and a top insulator.

10 Claims, 5 Drawing Sheets



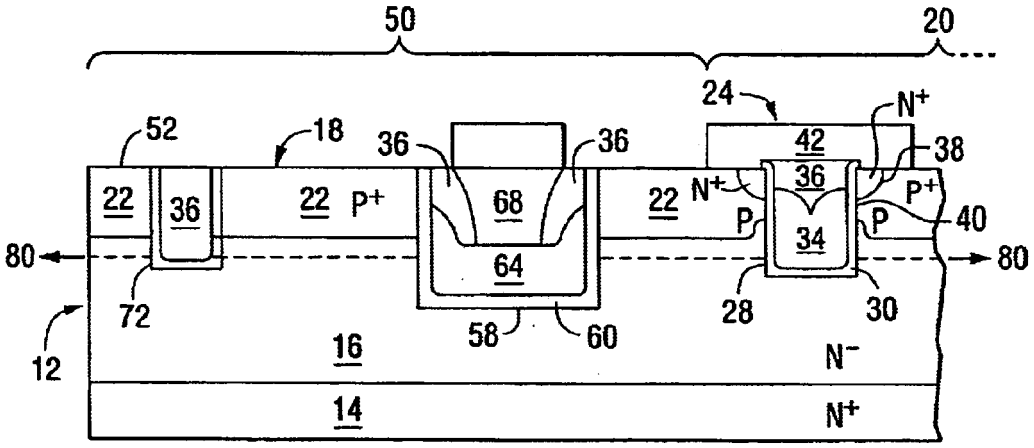


FIG. 1 10

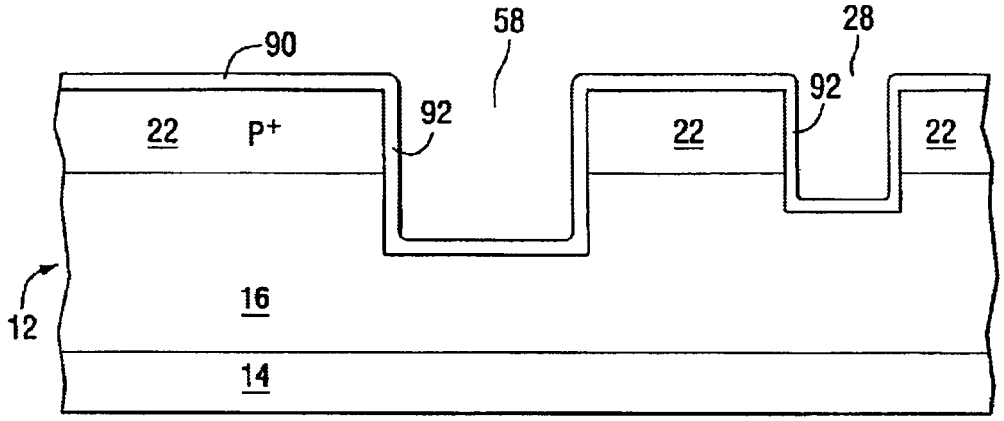


FIG. 3A

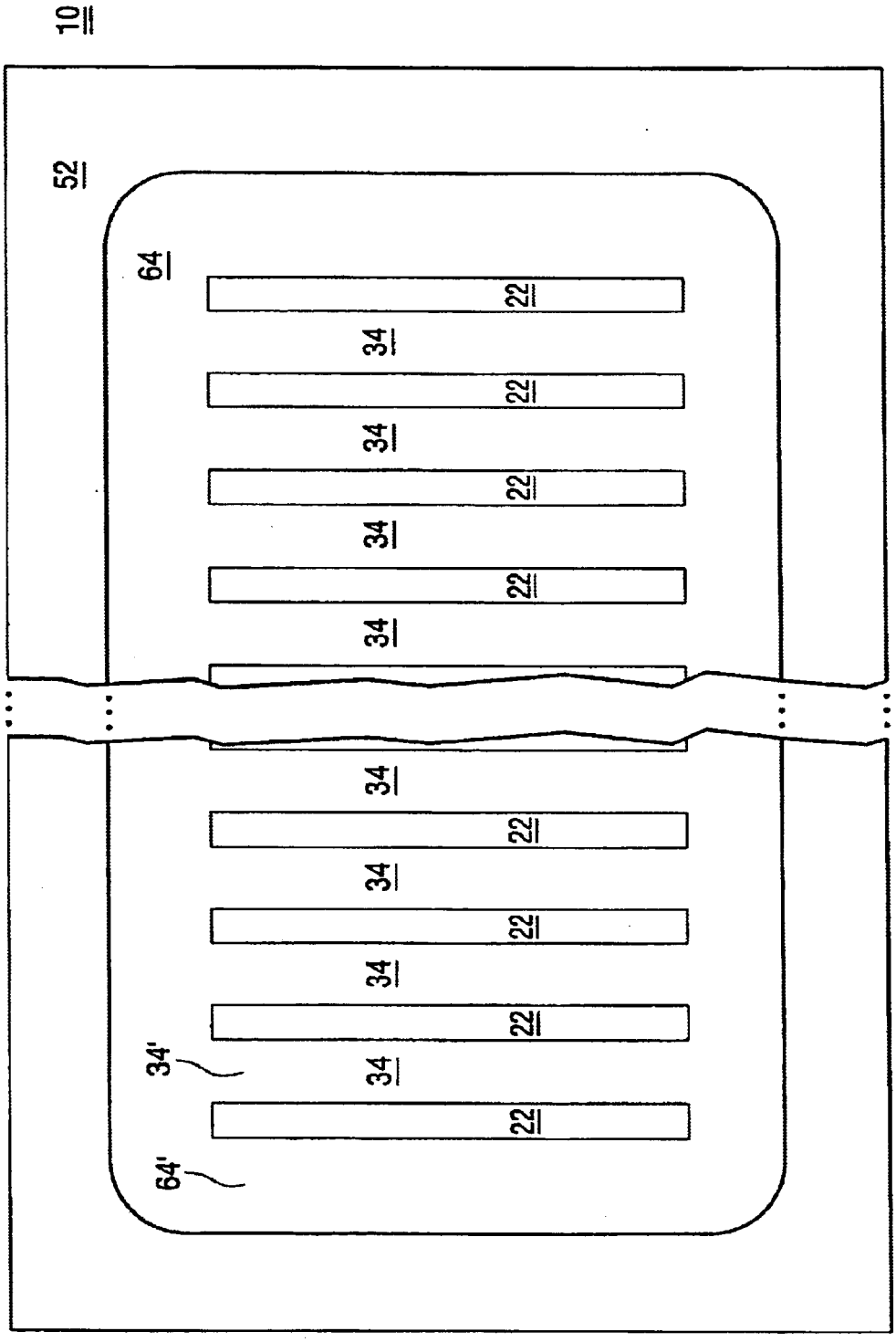


FIG. 2

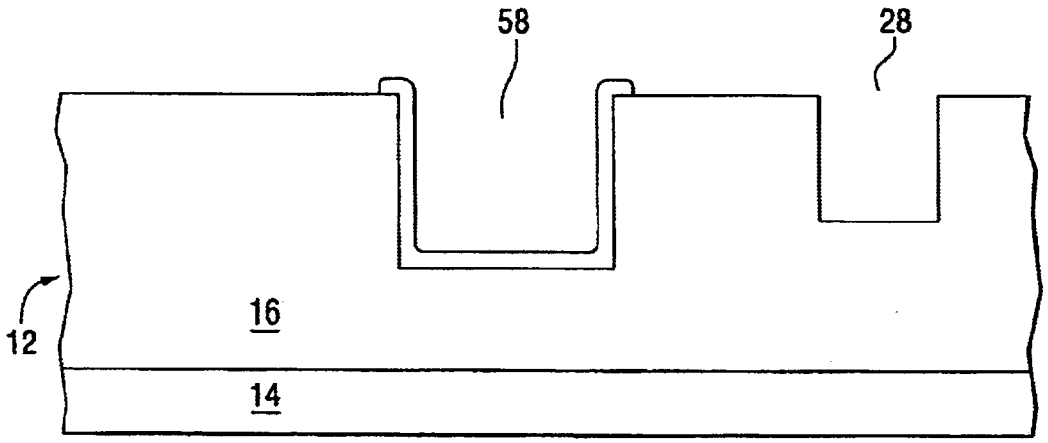


FIG. 3B

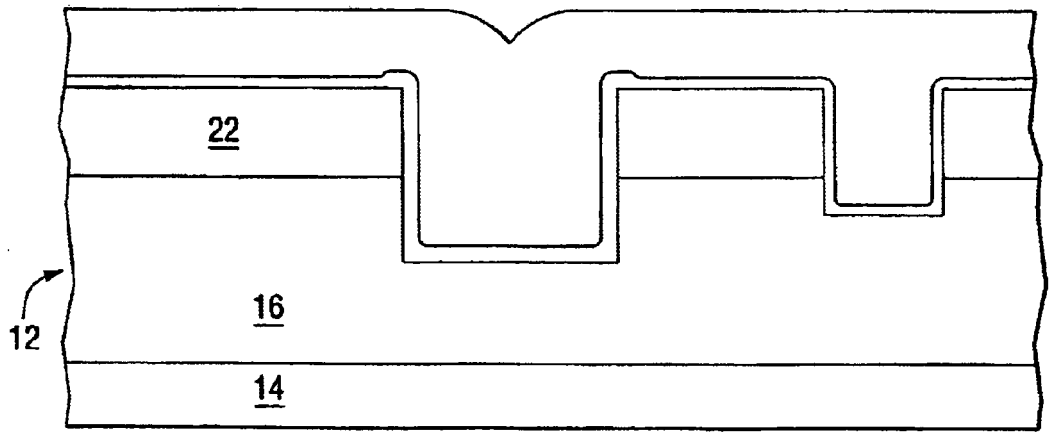


FIG. 3C

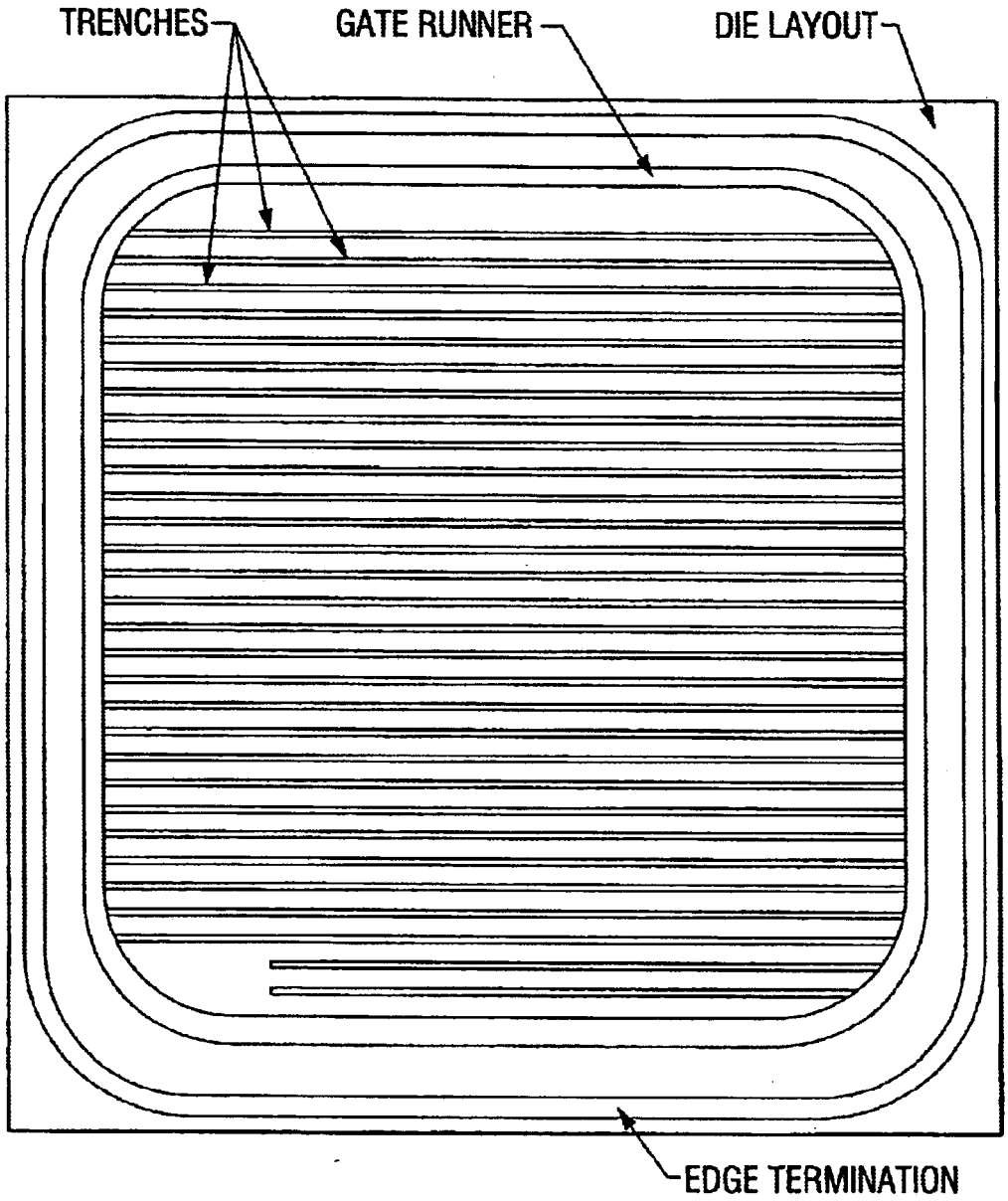


FIG. 4A

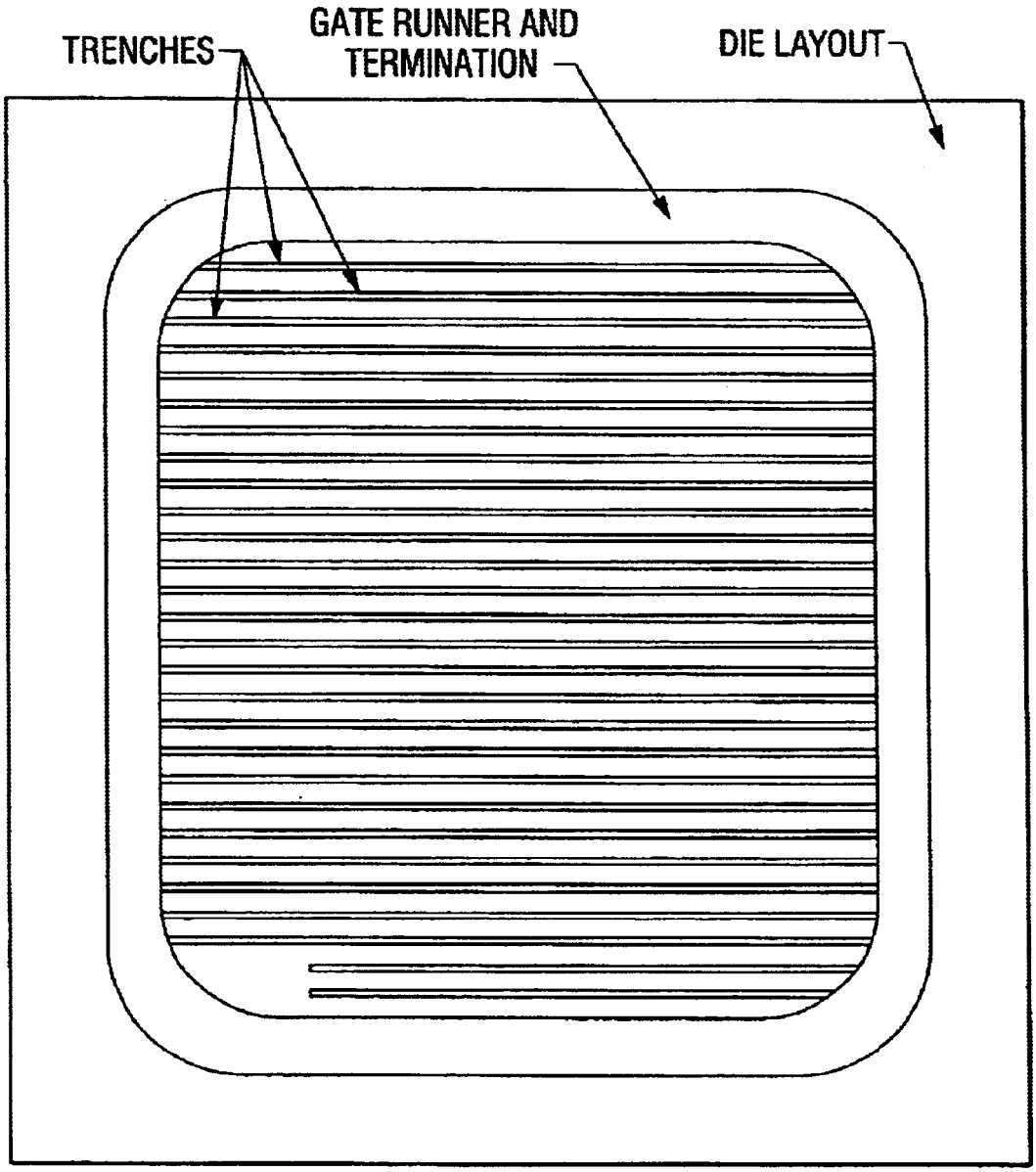


FIG. 4B

BURIED GATE-FIELD TERMINATION STRUCTURE

FIELD OF THE INVENTION

This invention relates to semiconductor devices and, more particularly, to semiconductor power devices and methods for fabricating such devices.

BACKGROUND OF THE INVENTION

There continues to be a growing demand for power switching devices, i.e., transistor devices capable of carrying large currents at high voltages. Such devices include bipolar and field effect devices including, for example, the Insulated Gate Bipolar transistor (IGBT) and the Metal Oxide Semiconductor Field Effect Transistor (MOSFET). Desirable characteristics of such devices include low on-resistance, fast switching speeds and low current draw during switching operations. That is, it is desirable to switch from an "off" state to an "on" state by applying a bias voltage to the gate electrode while experiencing only a small amount of current flow based on minimal capacitance inherent to the gate structure.

Notwithstanding significant advances in power device technologies, there remains a need to provide still higher-performing and more cost-efficient devices. For example, it is desirable to further increase current density relative to the total die area of a device. One of the limiting factors to higher current ratings is the breakdown voltage, particularly in the edge termination region. That is, because semiconductor junctions are not infinitely parallel, but include curvature, numerous techniques are employed to avoid otherwise high concentrations of electric field lines. Absent inclusion of so-called edge-termination designs, e.g., field rings, channel stop implants and field plates, to overcome degradation in the breakdown voltages, it would not be possible to approach the theoretical breakdown voltage of a semi-infinite junction. However, it is undesirable that, conventionally, a significant portion of the device die area must be devoted to edge termination designs in order to address this problem.

Breakdown voltage phenomena are well understood and the literature is replete with examples of edge termination designs. See, for example, see Ghandhi, *Semiconductor Power Devices*, John Wiley & Sons, Inc., 1977 (ISBN 0-471-029998), incorporated herein by reference, which discusses this subject at chapter two. See, also, Baliga, *Modern Power Devices,* Krieger Publishing Company, Malabar, Fla., 19920 (ISBN0894647997), also incorporated herein by reference, which provides relevant discussion at chapter three. In addition to conventional field rings and field plates, trenched field plates have been considered for edge termination applications. U.S. Pat. No. 5,233,215 discloses use of one or more trenched, floating field plates in combination with field rings in order to terminate a silicon carbide MOSFET. U.S. Pat. No. 5,578,851 discloses field rings separated by trenches, allowing the field rings to be closely spaced in order to conserve area. The trenches may be filled with polysilicon electrically connected to the MOSFET gate electrode. Nonetheless trench termination structures continue to occupy significant portions of the device die area and there is a need to provide termination techniques which are more area efficient. It is also desirable to reduce the manufacturing costs associate with high voltage performance. These and other benefits will be apparent from the invention that is now described.

SUMMARY OF THE INVENTION

An improved semiconductor power device is now provided. In one embodiment of the invention the device includes a semiconductor layer having a transistor region including a source/drain formation and a termination region surrounding the transistor region. The termination region includes an outer periphery corresponding to an edge of the device. A conductor, configured for connection to a voltage supply, includes first and second conductor portions. The first conductor portion is positioned in the transistor region to control current flow through the source/drain formation and the second conductor portion is positioned in the termination region. The second conductor portion includes a contact for connection to the voltage supply and a feed comprising conductive material formed in a trench extending along the outer periphery and around the transistor region. The feed portion electrically connects the contact portion with the first conductor portion.

An exemplary device according to the invention includes a layer of semiconductor material having an active device region and a peripheral region surrounding the active region. A transistor device formed in the active region has a gate region including a gate conductor formed in a trench. The gate conductor is electrically isolated from the semiconductor layer by a relatively thin insulator. A second trench is formed along the peripheral region and includes a second conductor formed therein with a relatively thick insulator positioned to electrically isolate the second trench conductor from the semiconductor layer.

An associated method for manufacturing a semiconductor device includes providing on a layer of semiconductor material an active region and a termination periphery region surrounding the active region with a trenched transistor formation in the active region. A trenched gate runner is formed in the termination region along the active region.

A method for operating a semiconductor device includes providing a semiconductor layer with an active transistor region and a trenched field plate positioned about the transistor region for increasing breakdown voltage. The field plate operates as a conductive feed to control switching of transistors in the active region. As such, the invention reduces the number of elements needed to make a power transistor by combining the gate runners and the field plate into one structure. The invention thus reduces the number of steps needed to make a device. Likewise, it increases the effective useable area of substrate so that substrates made with the invention can handle larger currents.

BRIEF DESCRIPTION OF THE DRAWINGS

The invention will be more fully understood when the following detailed description is read in conjunction with the drawings wherein:

FIG. **1** is a partial view in cross section of a semiconductor device incorporating the invention;

FIG. **2** is a plan view taken of the FIG. **1** device;

FIGS. **3**A–**3**C illustrate a sequence of fabrication steps according to the invention;

FIGS. **3**A–**3**C illustrate a sequence of fabrication steps according to the invention;

FIG. **4**A is a to view of prior art using planar edge termination and gate runner structures;

FIG. **4**B is a to view of the invention using buried termination and gate runner structures.

In accord with common practice the various illustrated features in the drawings are not to scale, but are drawn to

emphasize specific features relevant to the invention. Moreover, the sizes of features and the thicknesses of layers may depart substantially from the scale with which these are shown. Reference characters denote like elements throughout the figures and the text.

DETAILED DESCRIPTION OF THE INVENTION

The partial cross sectional view of FIG. **1** illustrates a P-channel MOSFET device **10** formed in a semiconductor layer **12**, including N+ lower layer **14** and N− upper layer **16** which may, for example, be epitaxially grown. The layer **16** has an upper surface **18**. A P+ diffusion region **22** extends from the surface **18** into the upper layer **16**. An active transistor region **20** of the device **10** (right side of drawing) includes a repetitive pattern of MOS cell structures each having a vertical source/drain formation. For simplicity of illustration only one exemplary MOSFET cell **24** is shown extending through a body region portion of the diffusion region **22**. The device **10** will include many MOSFET cells, although the specific design of the cell **24** is exemplary the invention is not at all limited to any particular type of cell design nor limited solely to MOSFET devices.

The cell **24** comprises a trench **28**, conventionally lined with a thermally grown gate oxide layer **30** having thickness in the range of 800 to 1200 Angstroms (80 to 120 nm). The trench may have a depth on the order of 1.5 to 3 microns with a width of one to two microns and is substantially filled with conductive material, e.g., doped polysilicon, to form a conductive gate electrode **34**. The balance of the trench opening is conventionally filled with deposited insulator **36** which may, for example, be borophosphorosilicate glass (BPSG). N+ source region **38** is formed along the surface **18** in an upper portion of the layer **16** surrounding the trench **28**. Lightly P-doped channel region **40** is formed in the otherwise more heavily doped diffusion region **22**, between the source region **38** and that portion of the N− layer **16** along the trench **28** which forms the drift region of the cell **24**. The oxide layer **30** provides electrical isolation between the gate electrode **34** and each of the source region **38**, channel region **40** and N− layer **16** (drain), allowing a conductive inversion layer to form in the channel region **40** when a voltage is applied to the gate electrode **34** relative to the source region **38**. A source contact **42**, e.g., **A1**, is provided for connection to the P+ region **22** as well as the source region **38** in order to suppress parasitic NPN bipolar effects which could occur under forward bias conditions, i.e., with the combination of the N+ region **38**, the P+ region **22** and the N-type layers **14** and **16**.

Still referring to FIG. **1**, a termination region **50** (left side of drawing) extends from the active region **20** to the outer periphery **52**, i.e., the die edge, of the device **10**. A gate runner trench **58** having depth and width substantially larger than that of the trench **28** is formed through the P+ region **22** in the termination region **50**. It may, for example, be 3 to 6 microns deep and 3 to 5 microns wide, but the trench **58** could be made substantially larger based on the desired device characteristics. The trench **58** is lined with a relatively thick insulative layer **60**, e.g., 1.5 or more times the thickness of the gate oxide layer **30** and, preferably, at least 300 to 500 nm.

Preferably, initial portions of the insulative layer **60** are formed before the gate oxide layer **30** is formed, but the layer **60** may include the thermally grown layer **30** as a component thereof. Preferably the insulative layer **60** predominantly comprises thermally grown or deposited silicon oxide, but may be formed with other dielectric materials. The trench **58** is substantially filled with conductive material **64**, and if this is the same deposit of doped polysilicon which forms the conductive gate electrode **34**, then the gate electrode **34** and the conductive material **64** will be integrally formed and a continuous layer, although they each may retain different functionalities. The remaining upper portion of the trench **58** is lined with the deposited insulator **36**, e.g., BPSG and a metal contact **68**, preferably Al, is formed thereover.

The diffusion region **22** extends from the active region **20**, through the termination region to the die edge. An isolation trench **72**, which may be formed at the same time as the trench **28**, includes the thermally grown oxide layer **30** and the deposited insulator **36**, preferably BPSG.

FIG. **2** is a simplified plan view of the device **10** taken along the cut-line **80** of FIG. **1**, illustrating a combination of an exemplary pattern of the trenched conductive material **64** and an exemplary pattern the trenched gate electrode **34**. For the FIG. **2** embodiment the partial view of FIG. **1** corresponds to a cross section taken through an end-most trenched gate electrode **34**, referenced in the drawing as **34'** and through the adjacent portion of the conductive material **64**, referenced in the drawing as **64'**. It should be recognized that, for each illustrated gate electrode **34** in FIG. **2**, there is a corresponding MOS cell structure (not illustrated in FIG. **2**) such as a MOSFET cell **24**. For purposes of illustration the gate electrodes **34** of only a few trenches **28** of the device **10** are shown, and neither the outline of the trenches **28** nor the gate oxide layers **30** are shown in FIG. **2**. A typical power device may include many more trenched gate electrodes than illustrated in the figures.

In the FIG. **2** embodiment the trenched conductive material **64** extends along the die edge **52** to provide a field plate termination. The isolation trench **72** (not shown in FIG. **2**) may also extend along the die edge **52**. With a metal contact (such as the contact **68** of FIG. **1**) connecting a gate voltage supply with the conductive material **64**, the conductive material **64** may be integrally formed in connection with the gate electrodes **34** to feed the gate signal to each MOSFET cell **24**. Thus the trench **58** with conductive material **64** also serves as the gate runner, in order to feed the external gate supply to each of multiple electrodes **34**. A feature of the invention is provision of one trenched conductor to serve as both a field plate and a gate runner to the several MOS cells in a device structure.

An exemplary method of making the device **10** is illustrated in FIGS. **3A–3D**, showing primarily those steps relevant to formation of the trenches **28** and **58**. Other conventional steps and process details for formation of power switching devices are not described as these will be readily apparent to those skilled in the art.

With reference to FIG. **3A**, the method for fabricating the device **10** is illustrated beginning with the semiconductor layer **12** shown to have the N+ lower layer **14** and N− upper layer **16** formed therein. A conventional P+ implant has been made through the surface **18**, and is shown after diffusion to create the P+ region **22**. A low-temperature silicon oxide **90** is formed over the eventual surface **18** followed by a conventional pattern and etch to form the trenches **28** and **58**. If it is desired to have the trenches **58** extend deeper into the layer **12**, e.g., substantially further into the N− upper layer **16** than the trenches **28**, then separate pattern and etch steps are had to create this feature. The trenches are shown lined with a sacrificial thermal oxide layer **92**.

Referring next to FIG. **3B**, once the trenches are defined, it is preferable to simultaneously remove both the low-

temperature oxide layer **90** and the sacrificial thermal oxide layer **92**, e.g., by a wet etch. Next, the trenches **28** are masked so that the thick layer **60** of silicon oxide, e.g., deposited by chemical vapor deposition (CVD), is selectively formed in the trenches **58** without formation of the same oxide in the trenches **28**. Alternately, the thick oxide layer **60** may be formed overall and selectively removed from the trenches **28** by a pattern and etch process.

After the thick oxide layer **60** is defined in the trench **58** (and subsequent to removal of any masking from over the trenches **28** or **58**, the high quality thermal gate oxide layer **30** is grown to a thickness on the order of 100 nm. Although the gate oxide layer **30** is intended primarily for formation in the trenches **28**, it may also be formed in the trenches **58** to add to the thickness of the layer **60**. The interim structure is shown in FIG. **3**C with a polysilicon layer **96** deposited by CVD, which is subsequently patterned to form the gate electrode **34** and conductive material **64** of trench **58** as shown in FIG. **1**. Subsequent process steps are conventional and need not be separately illustrated to describe the formation of other features shown in FIG. **1**. After formation of the contacts **42** and **68** as shown for the structure of FIG. **1** conventional insulator is applied over the exposed surface.

An advantage of the invention is that the edge termination feature, e.g., the trench **58**, need not be separately formed. Rather, definition of a termination trench with the same lithography steps as the trench **28** avoids raised topology effects which can otherwise obscure smaller feature definition. With the invention it is now possible to reduce the spacing between the active trenches **28** and the termination region **50** without experiencing adverse lithographic effects such as a reduction in the width of a trench **28** formed immediately next to a trench **58**.

FIG. **4**A shows a top view of the prior art using planar edge termination and gate runner structures. FIG. **4**B shows the ton view of the invention using buried termination and gate runner structures. By integrating the termination structure with the gate runner structure there is a reduction in the total die area required to effect both of these functions. For example, the distance from the die edge periphery **52** to the first active trench **28** may be about 20 microns, while for a device of similar rating but with a conventional edge termination structure, the distance from the edge of the die to the first active trench will be on the order of 120 microns. Also, having the termination region **50** include a portion of region **22** there is no need for a separate implant step, this resulting in a reduction in the number of processing steps required for manufacture of the device. With the termination structure formed in a trench that is simultaneously formed with the gate oxide trench, the overlying surface topography is planar, i.e., not characterized by steps due to oxide formation, and this avoids puddling of photoresist which is known to compromise lithographic image integrity.

Generally, the invention enables a higher breakdown voltage at the die edge with a reduced number of process steps. Although the invention has been described for a particular device type, the concepts apply to edge termination design for a wide variety of devices types and there is no limit on the voltage range of devices with which the invention may be practiced. The design principles may be readily applied to prevent breakdown voltages well in excess of 200 volts.

An architecture and process have been described for an improved semiconductor device. Exemplary embodiments have been disclosed while other embodiments of the invention, including structures composed of compound semiconductor materials, will be apparent. It is also to be understood that when a layer has been described or illustrated as positioned on or over another layer, there may be another intervening layer (not illustrated) associated with the same or an alternate embodiment of the invention. Moreover, although the invention has been illustrated for one set of conductivity types, e.g., N channel devices, application of the invention is contemplated for opposite conductivity-type devices as well. Because the invention may be practiced in a variety of ways, the scope of the invention is only limited by the claims which now follow.

We claim:

1. A switchable semiconductor power device of the type which controls current conduction based on field effect principles, comprising:

a semiconductor layer having a transistor region including a source/drain formation and a termination region surrounding the transistor region, said termination region including an outer periphery corresponding to an edge of the device; and

a single conductor, configured for connection to a gate voltage supply, including first and second conductor portions with the first conductor portion formed in a trench and being positioned in the transistor region to control current flow through the source/drain formation and the second conductor portion positioned in the termination region, the second conductor portion:

including a contact for connection to the gate voltage supply; and

including a feed comprising conductive material formed in a trench extending along the outer periphery and around the transistor region, said feed electrically connecting the contact with the first conductor portion; and acting as a field plate to extend the device breakdown voltage in the termination region; and

an isolation trench extending into the semiconductor layer and positioned between the edge of the device and the second conductor portion.

2. The device of claim **1** further comprising a plurality of additional source/drain formations each configured with the first conductor portion in and about a trench region to provide a voltage-switchable conduction channel for controlling current flow through the semiconductor layer.

3. The device of claim **1** wherein the transistor region comprises a vertical MOSFET device.

4. A method for manufacturing a semiconductor device, comprising:

providing on a layer of semiconductor material an active region and a termination periphery region surrounding the active region with a trenched transistor formation in the active region;

forming a trenched gate runner in the termination region along the active region; and

forming first and second conductor regions such that said first and second conductor regions are electrically connected to form a continuous conductor with multiple regions and said first conductor region is in said trenched transistor formation and said second conductor region is said trenched gate runner such that said second conductor also acts as a field plate termination; wherein

the trenched gate runner extends further into the layer of semiconductor material than the trenched transistor formation.

5. A method for manufacturing a semiconductor device, comprising:

providing on a layer of semiconductor material an active region and a termination periphery region surrounding the active region with a trenched transistor formation in the active region;

forming a trenched gate runner in the termination region along the active region, the trenched transistor formation including a gate conductor formed simultaneously with the gate runner by deposition of polysilicon; and

forming first and second conductor regions such that said first and second conductor regions are electrically connected to form a continuous conductor with multiple regions and said first conductor region is in said trenched transistor formation and said second conductor region is said trenched gate runner such that said second conductor also acts as a field plate termination

the trenched transistor formation including a gate conductor formed simultaneously with the gate runner by deposition of polysilicon

6. A semiconductor structure comprising:

a layer of semiconductor material having an active device region and a peripheral region surrounding the active region;

a transistor device formed in the active region including a plurality of source regions on one surface and drain region on the opposite surface;

a trench having an outer annular portion disposed in the peripheral region and enclosing the transistor device, the walls and the floor of the outer annular portion lined with an insulator and the outer annular portion filled with conductive material for forming a field plate around the transistor regions; and

a plurality of elongated inner runners extending in the same direction across the one surface with the source regions and intersecting the outer annular portion at opposite ends of the runners, the runners having their floors and their walls lined with a gate insulating material and the runners filled with a conductor

to form a gate structure in the transistor region to control current between the source regions and the drain.

7. The semiconductor of claim **6**, wherein the conductor material comprises conductive polysilicon.

8. The semiconductor of claim **7**, further comprising a layer of metal on the conductive polysilicon.

9. The semiconductor of claim **7** wherein the insulator in the outer annular portion is thicker than the gate insulator in the runners.

10. The semiconductor of claim **7** wherein a common layer of conductive polysilicon fills the trench.

* * * * *

UNITED STATES PATENT AND TRADEMARK OFFICE

CERTIFICATE OF CORRECTION

PATENT NO. : 6,818,947 B2
DATED : November 16, 2004
INVENTOR(S) : Thomas E. Grebs et al.

It is certified that error appears in the above-identified patent and that said Letters Patent is hereby corrected as shown below:

Column 1,
Line 55, replace "trenched" with -- trenches --

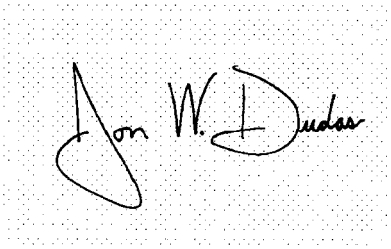
Column 2,
Lines 62 and 64, replace "to" with -- top --

Column 4,
Line 64, replace "are had" with -- can be used --

Column 5,
Line 36, replace "ton" with -- top --

Signed and Sealed this

Twenty-ninth Day of March, 2005



JON W. DUDAS
Director of the United States Patent and Trademark Office

EXHIBIT CC

TOWNSEND
and
TOWNSEND
and
CREW
LLP

San Francisco

Two Embarcadero Center
Eighth Floor
San Francisco, California 94111-3834
Tel 415.576.0200
Fax 415.576.0300

Direct: (415) 273-7511
mrhulse@townsend.com

August 25, 2008

VIA EMAIL AND U.S. FIRST CLASS MAIL

Harry F. Doscher
Morgan Lewis & Bockius LLP
2 Palo Alto Square
3000 El Camino Real, Suite 700
Palo Alto, CA 94306

Re: *Alpha & Omega Semiconductor v. Fairchild Semiconductor*
USDC N.D. CA Case No. C07-02638 JSW (EDL)
Consolidated with Case No. C07-02664 JSW
Our Reference No. 18865P-021600

Dear Harry:

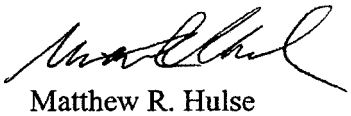
I write in response to your August 18, 2008, letter to Igor Shoiket concerning Fairchild's request for AOS's in-line data. Your letter is filled with inaccurate assertions. You claim that Fairchild "has never shown an interest" in the production of in-line data, for example. Yet Fairchild sought this data long ago. AOS's in-line data is responsive to at least Request Nos. 1, 3, and 8 in Fairchild's First Set of Requests for Production of Documents, which we served more than a year ago. We requested this data again on July 11, 2008. (Letter from Hulse to Hoffman, July 11, 2008, ("in-line data . . . must be produced for every AOS product."). There are other inaccuracies in the letter which I will not spend time addressing now.

In any event, we reject your request to withhold all of AOS's in-line data from discovery in this case. In-line data is collected during the manufacturing process, and typically includes information concerning the structural features of devices. Accordingly, certain in-line data is highly relevant to infringement issues in this case, as many asserted claims of the Fairchild Mo patents include limitations directed to structural aspects of devices, including the depths of trenches, doped wells, and other features. *See, e.g.*, claim 1 of the '481 patent. Additionally, in-line data can be used as input information for simulations of AOS's accused products.

AOS objects to the production of in-line data on the grounds that it is irrelevant and unduly burdensome to produce. We disagree. As for relevance, for the reasons explained above, certain in-line data is highly relevant to infringement issues presented by the Fairchild patents. We are willing to work with AOS to reduce the burden this production may impose. But AOS's

prior proposal regarding quality control data is unacceptable to the extent it would potentially exclude from production certain categories of relevant data, including some listed above. Nevertheless, there is some in-line data that may be excluded from production. AOS produced two spreadsheets after we filed the motion to compel which you represented in your August 18, 2008, letter were samples of AOS's quality assurance documents. AOS can exclude from production these spreadsheets for all AOS products. However, AOS should produce other categories of in-line data, including trench measurements, field oxide measurements, gate oxide measurements, poly gate measurements, and other measurements relating to the structure of AOS's accused products. We are willing to consider any proposals AOS may have to reduce the burden of producing such data.

Very truly yours,



Matthew R. Hulse

61476915 v1